Bluetooth Module Datasheet

Model: AR-7109T

Version: V1.0

2022-02-15

Shenzhen Every Interconnect Technologies Co., Ltd.

TEL: (0755)23410907

Fax: (0755)23410907

E-mail: guang.ma@every-connect.com

Add: 4 / F, building D, Guangming Zhizao hi tech Industrial Park,

ZhenMeiCommunity, Xinhu Street, Guangming District, Shenzhen

Release Record

Version	Release Date	Comments
V1.0	2022-02-18	Init

List of Contents

1 Introduction

AR-7109T is a Bluetooth 5.1 dual-mode module that provides a system that is fully compatible with Classic Bluetooth (BR/EDR) and Bluetooth Low Energy (BLE), and can be used for Bluetooth audio and data communications.

AR-7109T uses a highly integrated SoC Bluetooth chip, integrated ultra-low power DSP, application processor, embedded flash memory, high-performance stereo codec, power management subsystem, I2S, LED driver and ADC I/O and other subsystems . The dual-core architecture with flash memory allows manufacturers to easily use new features for differentiated development of their products without extending the development cycle.

By default, the AR-7109T module is equipped with powerful and easy-to-use Reddy firmware. Reddy firmware enables users to pass simple ASCII commands to the module through the serial interface to access Bluetooth functions, just like a Bluetooth modem.

Therefore, AR-7109T provides an ideal solution for developers who want to integrate Bluetooth wireless technology into their designs.

1.1 System architecture

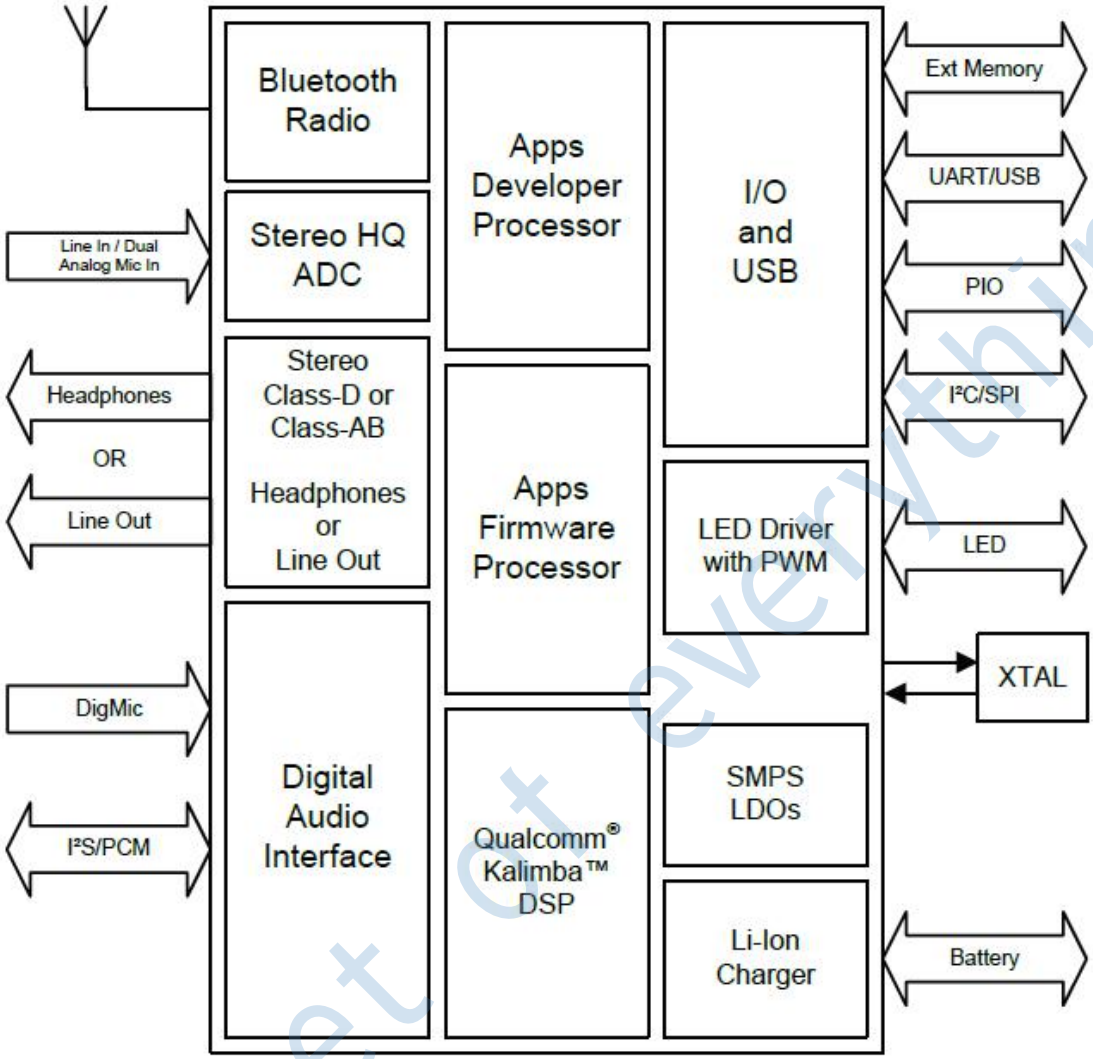


Figure 1: System architecture

1.2 Features

- Qualified to Bluetooth® v5.0 specification
- 120 MHz Qualcomm® Kalimba™ audio DSP
- 32 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- Advanced audio algorithms

- High-performance 24‑bit stereo audio interface
- Digital and analog microphone interfaces
- Flexible PIO controller and LED pins with PWM support
- 1 or 2-mic Qualcomm® cVc™ headset noise reduction and echo cancellation technology
- SBC and AAC audio codecs support
- aptX, aptX HD, aptX Low Latency, SBC, and AAC audio codecs support
- Serial interfaces: UART, Bit Serializer (I²C/SPI),USB 2.0
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- 90-ball 5.5 x 5.5 x 1.0 mm,0.5 mm pitch VFBGA

1.3 Device description

- High-performance programmable Bluetooth® stereo audio SoC with Qualcomm® aptX™ audio
- Fully qualified single-chip dual-mode Bluetooth v5.0 system
- Tri-core processor architecture with low power for extended battery life

1.4 Applications

- Wired/wireless stereo headsets/headphones
- Qualcomm TrueWireless™ stereo earbuds
- Bluetooth music box
- Car audio application

2 General Specification

Table 1: General Specification

Bluetooth Specification	
Standard	Fully qualified single-chip dual mode Bluetooth v5.0 , Class 1.5a
Chipset	QCC3034 VFBGA
Profiles	HS/HF, A2DP, AVRCP, SPP, etc. detailed profiles depends on the firmware
Frequency Band	2.402GHz ~ 2.480GHz
Maximum Data Rate	3Mbps
RF Input Impedance	50 ohms

Baseband Crystal OSC	26MHz
Interface	UART, PIO, AIO, USB, SPI, Speaker, Microphone, etc.
Sensitivity	-85dBm@0.1%BER
RF TX Power	7dBm
Power	
Supply Voltage	2.7V ~ 3.6V DC
Working Current	Depends on profiles
Standby Current	TBD
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Certifications	TBD
Environmental	TBD
Dimension and Weight	
Dimension	23.2mm x 11.9mm x 2.0mm
Weight	TBD

a) The maximum RF TX Power is 9dBm.

3 Pin Definition

3.1 Pin Configuration

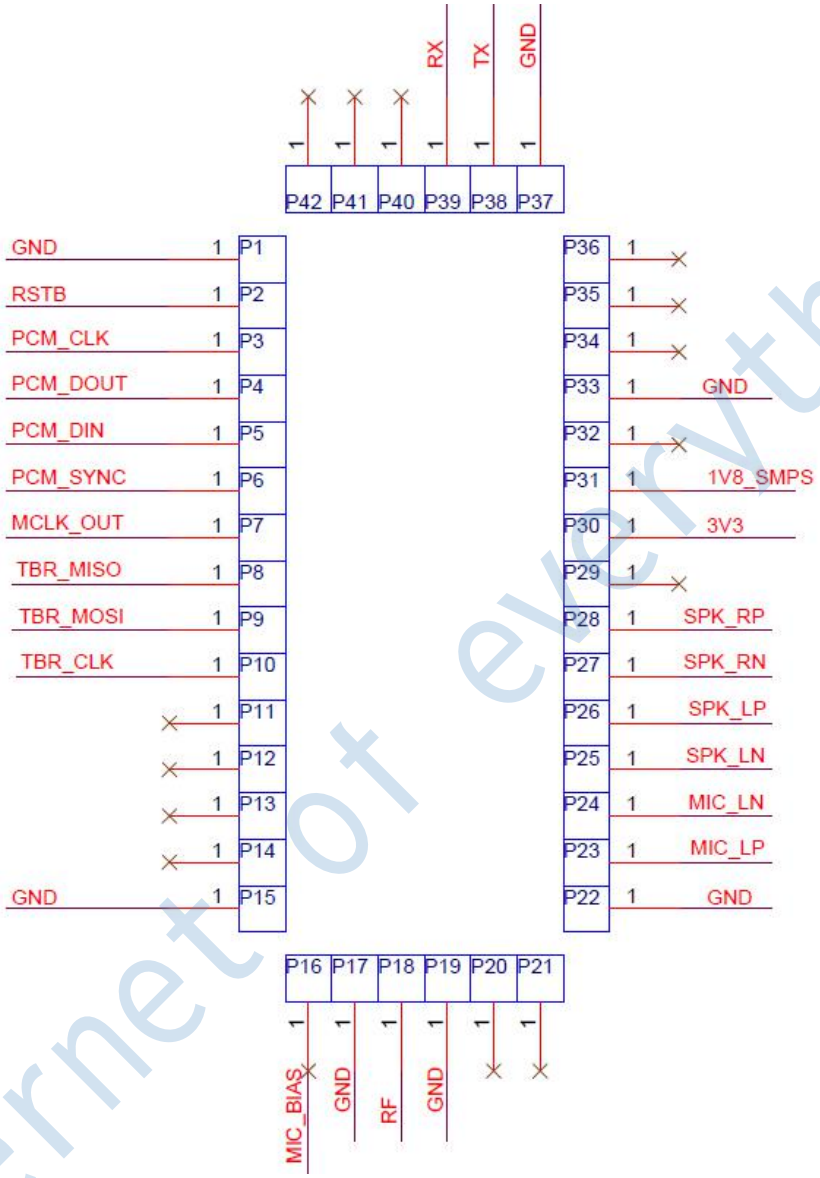


Figure 2: Pin Configuration

3.2 Pin Definition

Table 2: Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	RSTB	Input with strong pull-up	Reset if low. Pull low for minimum 5ms to cause a reset.

3	PCM_CLK	Bidirectional with weak pull-down	SPI_CLK: Debug SPI clock Alternative function:-I2S_SCK: I²S synchronous data clock
4	PCM_DOUT	Bidirectional with weak pull-down	SPI_MISO: Debug SPI data output Alternative function:- I2S_SD_OUT: I²S synchronous data output
5	PCM _DIN	Bidirectional with weak pull-down	SPI_MISO: Debug SPI data input Alternative function:-I2S_SD_IN: I²S synchronous data input
6	PCM _SYNC	Bidirectional with weak pull-down	SPI_CSB: chip select for Debug SPI, active low Alternative function: -I2S_WS:I²S word select
7	MCLK_OUT	Bidirectional with strong pull-down	Programmable input/output line Alternative function: - I2S2_WS:I²S2 word select
8	TBR_MISO	Bidirectional with weak pull-down	Programmable input/output line
9	TBR_MOSI	Bidirectional with strong pull-down	Programmable input/output line Alternative function: - I2S2_SD_SCK:I²S2 synchronous data clock -UART_CTS:UART clear to send, active low
10	TBR_CLK	Bidirectional with weak pull-down	Programmable input/output line
11	NC	NC	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	GND	Ground	Ground
16	MIC_BIAS	Analogue	Microphone Bias
17	GND	RF Ground	RF Ground
18	RF	Analogue	Bluetooth transmit/receive
19	GND	RF Ground	RF Ground
20	NC	NC	NC
21	NC	NC	NC
22	GND	Ground	Ground
23	MIC_LP	Analogue	Microphone input positive
24	MIC_LN	Analogue	Microphone input negative
25	SPK_LN	Analogue	Speaker output negative (left side)
26	SPK_LP	Analogue	Speaker output positive (left side)
27	SPK_RN	Analogue	Speaker output negative (right side)
28	SPK_RP	Analogue	Speaker output positive (right side)
29	NC	NC	NC
30	3V3	3.3v power input	3.3v power input

31	1V8_SMPS	Bidirectional	USB data plus with selectableinternal 1.5kpull-upresistor
32	NC	NC	NC
33	GND	Ground	Ground
34	NC	NC	NC
35	NC	NC	NC
36	NC	NC	NC
37	GND	Ground	Ground
38	TX	Bidirectional with strong pull-up	UART data output
39	RX	Bidirectional with strong pull-up	UART data input
40	NC	NC	NC
41	NC	NC	NC
42	NC	NC	NC

NOTE: Pin8 and pin10 are connected inside the module to accommodate the needs of old customers.

4 Physical Interfaces

4.1 Power

The transient response of the regulator is very important. If the power rail of the module is powered by an external voltage source, the transient response of any regulator used should be 20μs or less. The power rail must be restored quickly, which is critical.

4.2 RESETB

AR-7109T is reset from several sources:

- RESETB pin
- Power-on reset
- Software configured watchdog timer
- UART break character

The RESETB pin is an active low reset. Assert the reset signal for a period > 5 ms to ensure a full reset. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

Note: In the following cases, the reset can also be triggered by the UART interrupt symbol:

- Host interface is any UART transmission
- PSKEY_HOSTIO_UART_RESET_TIMEOUT is set to a value greater than 1000.

Under the control of the software, the restart function can also be used.

4.3 RF interface

For this module, you can choose built-in or external antenna. Users who choose external devices can connect the 50ohm antenna directly to the RF port.

- 2402–2480 MHz Bluetooth 5.1 dual mode (Classic BT and BLE); the air data rate is 1 Mbps to 3 Mbps.
- TX output power is +9dBm (MAX)
- The receiver can achieve maximum sensitivity -100dBm @ BLE or -97dBm @ Classic BT

4.4 UART Interface

AR-7109T provides a channel of Universal Asynchronous Receiver Transmitter (UART) (full-duplex asynchronous communication). The UART controller performs serial-to-parallel conversion on the data received from the peripheral, and performs parallel-to-serial conversion on the data transmitted from the CPU. Each UART controller channel supports ten types of interrupts.

This is a standard UART interface used to communicate with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The other two signals UART_CTS and UART_RTS can be used to implement RS232 hardware flow control, and two of them are low-level active indicators.

The output of this module is 3.3V CMOS logic level (tracking VCC). A level conversion must be added to connect to an interface that conforms to the RS-232 level.

Some serial implementations link CTS and RTS together to eliminate the need for handshaking. Except for testing and prototyping, we do not recommend linking CTS and RTS. If these pins are linked and the host sends data when the FSC-BT1026X deactivates its RTS signal, there is a huge risk of overflow of the internal receiving buffer, which may cause the internal processor to crash. This will disconnect and may require a power cycle to reset the module. We recommend that you follow the correct CTS / RTS handshake protocol to ensure normal operation.

Table: Possible UART settings

Table 3: Possible UART Settings

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 6 lists common baud rates and their associated error values for PSKEY_UART_BITRATE. To set the UART baud rate, load PSKEY_UART_BITRATE with the number of bits per second.

Table 4: Standard Baud Rates

Baud rate	PS Key value(bits per second)	Error
1200	1200	1.73%
2400	2400	1.73%
4800	4800	1.73%
9600	9600	-0.82%
19200	19200	0.45%
38400	38400	-0.18%
57600	57600	0.03%
76800	76800	0.14%
115200	115200	0.03%
230400	230400	0.03%
460800	460800	-0.02%
921600	921600	0.00%
1382400	1382400	-0.01%
1843200	1843200	0.00%
2764800	2764800	0.00%
3686400	3686400	0.00%

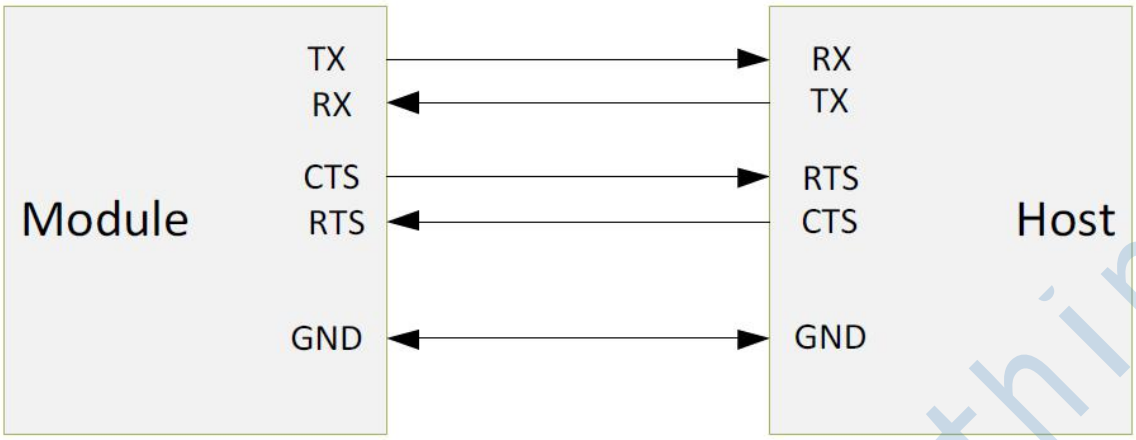


Figure 3

After receiving the interrupt signal, the UART interface resets the AR-7109T. The interrupt is identified by the continuous logic low level (0V) on the UART_RX terminal, as shown in the figure below. If tBRK is greater than the value defined by PSKEY_HOSTIO_UART _RESET_TIMEOUT, a reset will occur. This function allows the host to initialize the system to a known state. In addition, AR-7109T can send out an interrupt character to wake up the host.

Figure 4

When the AR-7109T remains in the reset state, the UART interface is tri-stated. This allows users to connect other devices to the physical UART bus. The limitation of this method is that when the AR-7109T reset is invalid, all devices connected to the bus must enter the tri-state and Audio Interface

4.5 Audio Interface

The audio interface circuit includes:

- Single analog microphone input and dual analog line input
- Dual analog audio output
- 1 digital microphone input

- 1 set of configurable I2S interface
- Configurable SPDIF input/output interface

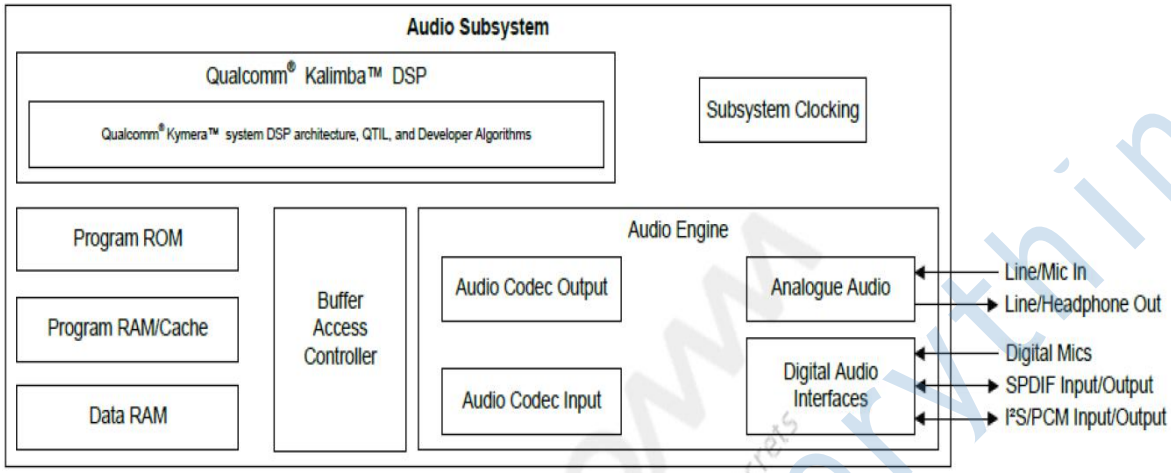


Figure 5

4.5.1 Audio input and output

The audio input circuit includes 2 independent 24-bit high-quality ADC channels:

- Programmable as stereo or dual mono input
- 1 input can be programmed as microphone or line input
- Each channel can be connected as single-ended or fully differential
- Each channel has an analog and digital programmable gain stage

The audio output circuit includes a dual differential Class A-B output stage.

Note: AR-7109T is designed for differential audio output. If single-ended audio output is required, use an external differential single-ended converter.

4.5.2 Audio codec interface

The interface has the following functions:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

Note: To avoid any confusion related to stereo operation, this data sheet clearly indicates the right channel of the left and right audio output. Regarding audio input, software and any registers, channel 0 or channel A represents the left channel, and channel 1 or B represents the right channel.

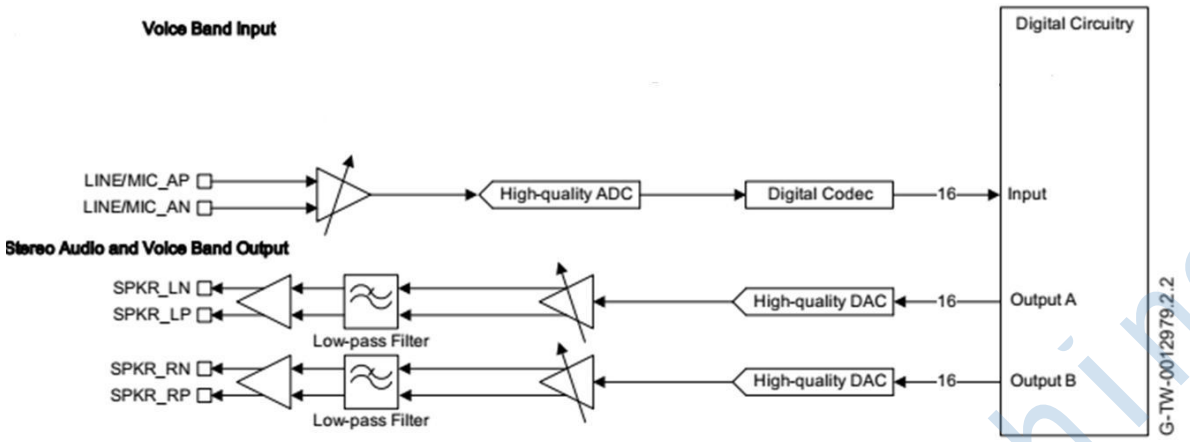


Figure 6: Audio Input and Output

The AR-7109T audio codec uses a fully differential architecture in the analog signal path. This architecture can reduce common-mode noise sensitivity and has good power supply rejection performance, while effectively doubling the signal amplitude. It uses dual power supply, the audio circuit is VDD_AUDIO (internal), and the audio driver circuit is VDD_AUDIO_DRV (internal).

4.5.3 ADC

AR-7109T contains 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is an independent channel with the same function.
- Each channel has an analog and digital gain stage.

4.5.4 ADC sampling rate selection

Each ADC supports the following predefined sampling rates, although other rates are programmable, such as 40kHz:

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz，48Khz，96 Khz.

4.5.5 ADC Audio Input Gain

The audio input gain consists of the following components:

- An analog gain stage based on a pre-amplifier and an analog gain amplifier.
- A digital gain stage.

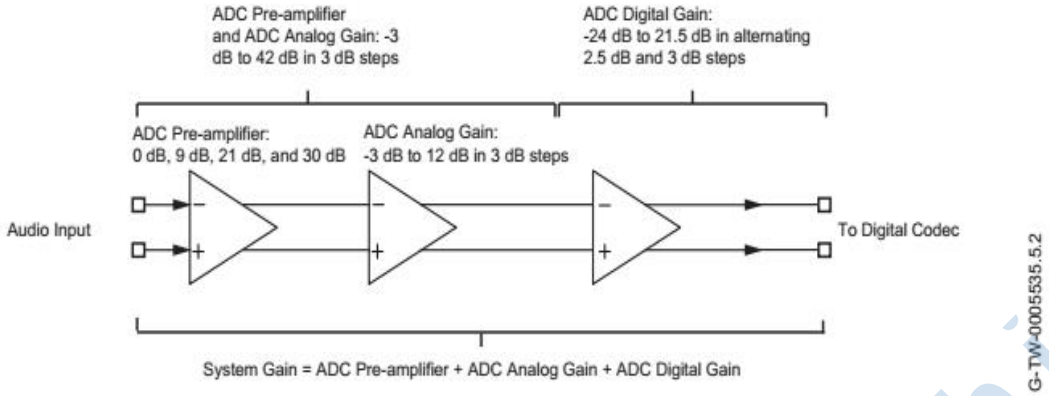


Figure 7: Audio Input Gain

4.5.6 ADC Pre-Amplifier And Analog/Digital Gain

The gain of the ADC inputs can be configured in the range of -27 dB to 63.5 dB steps, making it suitable for line and microphone input levels. 0 dB is 1600 mV pk-pk input.

The ADC input impedance is nominal 6 kΩ except when 0 dB pre-amplifier gain is selected when it becomes 12 kΩ.

If the input pre-amplifier is disabled, the input impedance varies between 6 k and 34 k depending on gain selection. In normal operation, the input pre-amplifier is enabled.

Calls connected by the VM stream automatically select the distribution of gain within the ADC for best performance. Alternatively, the individual gain stages can be set.

4.5.7 ADC Digital Gain

Table 5: ADC Audio Input Gain Selection

Digital Gain Selection Value	ADC Digital Gain Setting(Db)	Digital Gain Selection Value	ADC Digital Gain Setting(Db)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

4.5.8 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

A long IIR filter suitable for music (> 44.1 kHz).G.722 filter. This is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance. This filter is the best selection for 8 kHz/16 kHz/voice.

4.5.9 Microphone Bias Generator

AR-7109T contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones.

Figure 5 shows a typical biasing circuit for electret condenser microphones..

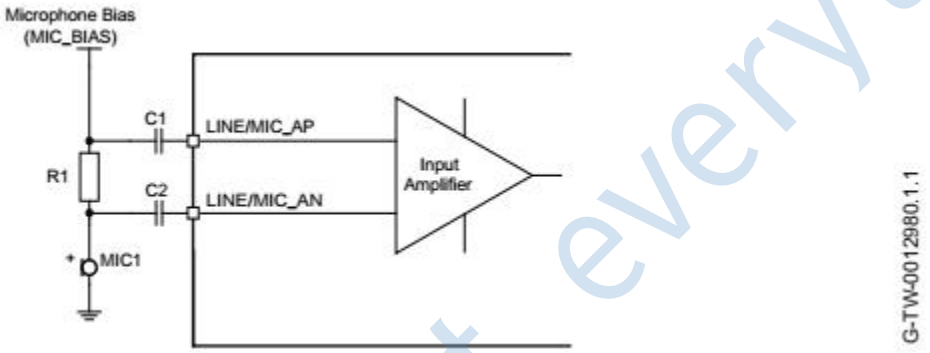


Figure 8: Micro phone Biasing

The microphone bias generator provides a selectable output voltage of 1.8 V or 2.6 V nominal.

No output capacitor is required.

4.5.10 Output Stage

The output stage digital circuitry converts the signal from 16 bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analog output circuitry.

The analog output circuit comprises a DAC, a buffer with gain-setting, a low pass filter, and a class AB output stage amplifier.

Figure 6 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

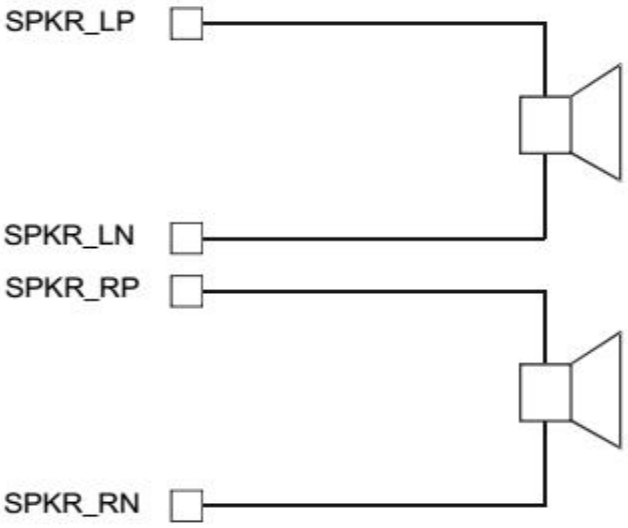


Figure 9: Speaker Output

4.5.11 Sidetone

In some applications, it is necessary to implement sidetone. This sidetone function applies configurable gain to the microphone signal and feeds it into the DAC stream. The sidetone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface

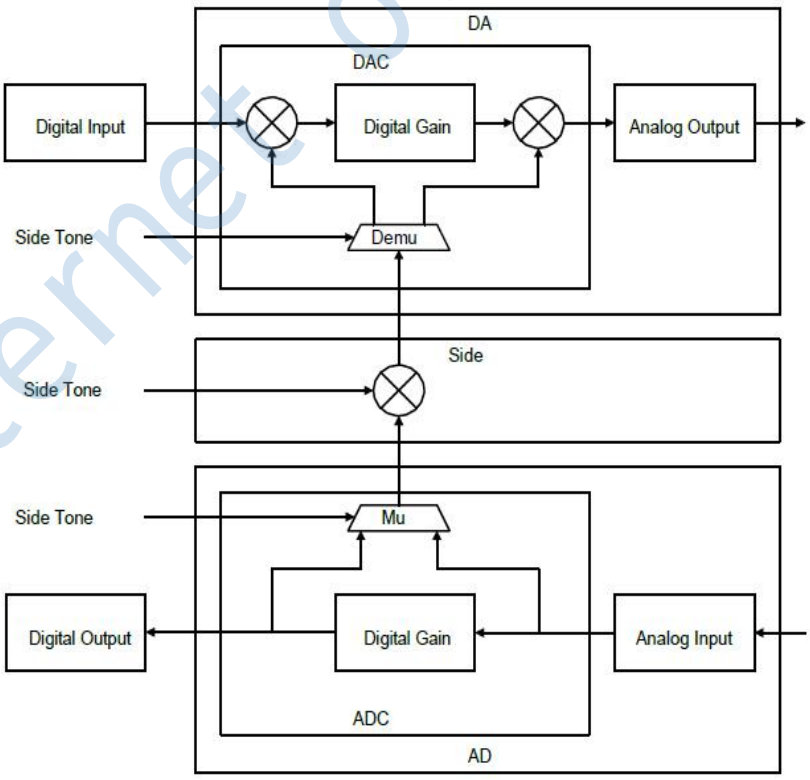


Figure 10: Sidetone

The ADC provides simple gain to the sidetone data. The gain values range from -32.6 dB to 12.0 dB in alternating steps of 2.5 dB and 3.5 Db

Table 6: Sidetone Gain

Value	Sidetone Gain(dB)	Value	Sidetone Gain(dB)
0	-32.6	8	-8.5
1	-30.1	9	-6.0
2	-26.6	10	-2.5
3	-24.1	11	0
4	-20.6	12	3.5
5	-18.1	13	6.0
6	-14.5	14	9.5
7	-12.0	15	12.0

4.5.12 Standard I²S/PCM interface

AR-7109T provides a standard I²S/PCM interface capable of operating at up to a 192 kHz sample rate.The I²S/PCM port is highly configurable, and has the following options:

Master (generate CLK and WS) or Slave (receive CLK and WS)

■ Word Select polarity

■ Left or right justification

■ Sign extension / zero pad

■ Optional 1‑bit period delay on WS to start of channel data

■ 13/16/24-bit per sample

■ Up to four slots per frame

NOTE In multislot operation with 3 or 4 slots per frame, data padding to 32 bits within slots is not possible.

AR-7109T also supports several alternative PCM data formats. When in PCM mode, the following pin name to function mappings apply.

I²S Pin	PCM Function
I2Sn_SD_IN	PCM_DIN
I2Sn_SD_OUT	PCM_DOUT
I2Sn_WS	PCM_SYNC
I2Sn_SCK	PCM_CLK

4.5.13 I²S/PCM master mode timing diagram

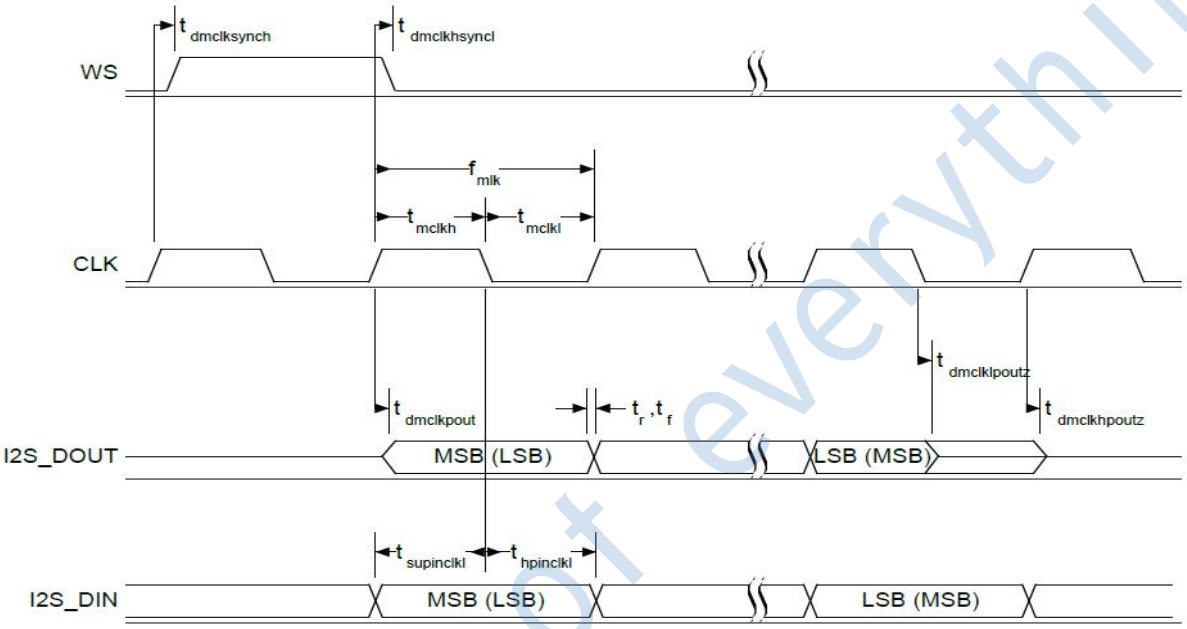


Figure 11: I²S/PCM master mode timing diagram

I²S/PCM master mode timing diagram symbols

Table 7: I²S/PCM master mode timing diagram symbols

Symbol	Parameter	Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from I2S_CLK high to I2S_SYNC high	_	_	20	Ns
$t_{dmclkpout}$	Delay time from I2S_CLK high to valid I2S_OUT	_	_	20	ns
$t_{dmclkhsyncl}$	Delay time from I2S_CLK high to I2S_SYNC low	_	_	20	ns
$t_{dmclklpoutz}$	Delay time from I2S_CLK low to I2S_OUT high impedance	_	_	20	ns
$t_{dmclkhpoutz}$	Delay time from I2S_CLK high to I2S_OUT high impedance	_	_	20	ns
$t_{supinclkl}$	Set-up time for I2S_IN valid to I2S_CLK low	_	_	20	ns
$t_{hpinclkl}$	Hold time for I2S_CLK low to I2S_IN invalid	0	_	_	ns

4.5.14 I²S/PCM slave mode timing diagram

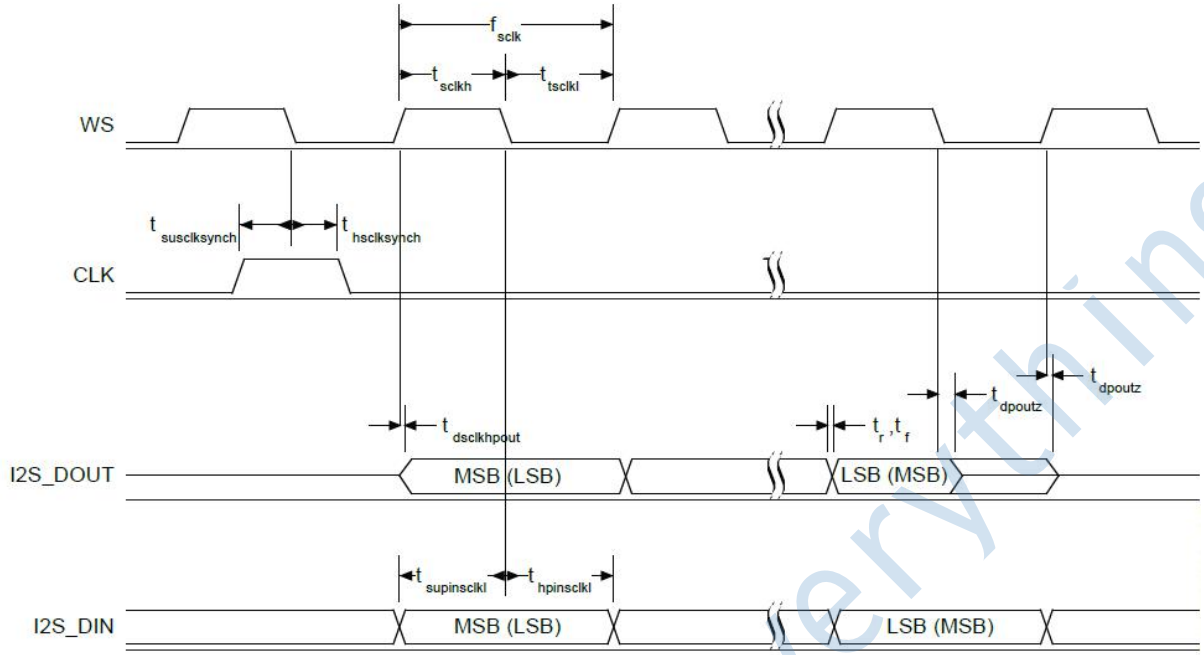


Figure 12: I²S/PCM master mode timing diagram

Table 8 I²S/PCM slave mode timing diagram symbols

Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from I2S_CLK low to I2S_SYNC high	5	_	_	ns
$t_{susclksynch}$	Set-up time for I2S_SYNC high to I2S_CLK low	15	_	_	ns
$t_{dsclkhpout}$	Delay time from CLK high to I2S_OUT validdata	_	_	20	ns
t_{dpoutz}	Delay time from I2S_SYNC or I2S_CLK low,whichever is later, to I2S_OUT data line high impedance	_	_	20	ns
$t_{supinsclkl}$	Set-up time for I2S_IN valid to CLK low	15	_	_	ns
$t_{hpinsclkl}$	Hold time for I2S_CLK low to I2S_IN invalid	5	_	_	ns

4.5.15 aptx Codec

The aptX audio codec is available for high-quality stereo audio over Bluetooth. When incorporated in Bluetooth A2DP stereo products, aptX audio coding delivers full wired audio quality. The aptX audio codec source material is delivered transparently over the Bluetooth link, whether it is stored uncompressed or in an alternative compression (AAC, FLAC) format.

The aptX codec has the following target applications:

■ Bluetooth stereo headphones/headsets
■ Bluetooth automotive audio
■ Bluetooth stereo speakers

The aptX codec has the following benefits:

■ Outstanding Bluetooth Stereo audio quality

■ Faithful reproduction of full audio bandwidth
■ Minimization of lip-sync issues via low-delay audio decoding techniques
■ Nondestructive transcoding from other standard coded audio formats
■ Low code memory and data memory requirements
■ A2DP-compliant negotiation back to the SBC codec when connecting with legacy audio sources
The aptX codec has the following key features:
■ Multiple audio sample rate support, including Fs = 44.1 kHz and Fs = 48 kHz
■ Conveyance of CD-quality audio (16-bit and Fs = 44.1 kHz) over Bluetooth at a data rate of 352 kbps
■ Frequency response maintained from 10 Hz to 22 kHz for Fs = 48 kHz
■ Algorithmic delay less than 1.89 ms for Fs = 48 kHz
■ Dynamic range for 16-bit audio in excess of 92 dB

5 Electrical Characteristic

5.1 Absolute Maximum Rating

Table 9: Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+85	°C
PIO/AIO Voltage	-0.4	3.60	V
VDD	-0.4	3.60	V
USB_DP/USB_DN Voltage	-0.4	3.60	V
Other Terminal Voltages except RF	-0.4	3.60	V

5.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	_	+85	°C
Operating Temperature Range	-40	_	+85	°C
VDD	+3.1	+3.3	+3.6	V
PIO	+1.7	+1.8	+3.6	V

5.3 Input/output Terminal Characteristics

5.3.1 Digital Terminals

Table 11: Digital Terminal

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				

VIL input logic level low	-0.4	_	+0.4	V
VIH input logic level high	0.7VDDIO	_	VDDIO+0.4	V
Tr/Tf	_	_	25	ns
Output Voltage Levels				
VOL output logic level low, lOL = 4.0mA	_	_	0.4	V
VOH output logic level high, lOH = -4.0mA	VDDIO-0.2	_	_	V
Tr/Tf	_	_	5	ns
Input and Tri-state Current				
With strong pull-up	-150	-40	-10	µA
With strong pull-down	10	40	150	µA
With weak pull-up	-5	-1.0	-0.33	µA
With weak pull-down	0.33	+1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA
CI Input Capacitance	1.0	_	5.0	pF

VDDIO is the supply domain for this i/o. Typical value is 1.8V.

5.3.2 Stereo Codec: Analog-To-Digital Converter

Table 12: Analog-To-Digital Converter

Analog-To-Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	_		_	_	16	Bits
Input sample rate,Fsample	_		8	_	48	kHz
Maximum ADC input signal amplitude	0dB =1600 mVpk-pk		13	_	2260	mVpk-pk
SNR	fin=1 kHz B/W=20Hz→Fsample/2(20kHz max) A- Weighted THD+N<0.1% 1.6Vpk-pk input	F_{sample}				
		8 kHz	_	94.4	_	dB
		16 kHz	_	92.4	_	dB
		32 kHz	_	92.5	_	dB
		44.1 kHz	_	93.2	_	dB
		48 kHz	_	91.9	_	dB
THD+N	fin= 1 kHz B/W=20Hz→Fsample/2 (20 kHz max) 1.6Vpk-pk input	F_{sample}				
		8 kHz	_	0.004	_	%
		48 kHz	_	0.016	_	%
Digital gain	Digital gain resolution = 1/32	-24	_	21.5	_	dB

Analog gain	Pre-amplifier setting =0 dB, 9dB, 21dB or 30 dB Analog setting =-3dB to12 dBin 3dB steps	-3	_	42	_	dB
Stereo separation (crosstalk)			_	-89.9	_	dB

5.3.3 Stereo Codec: Digital-To-Analog Converter

Table 13: Digital-To-Analog Converter

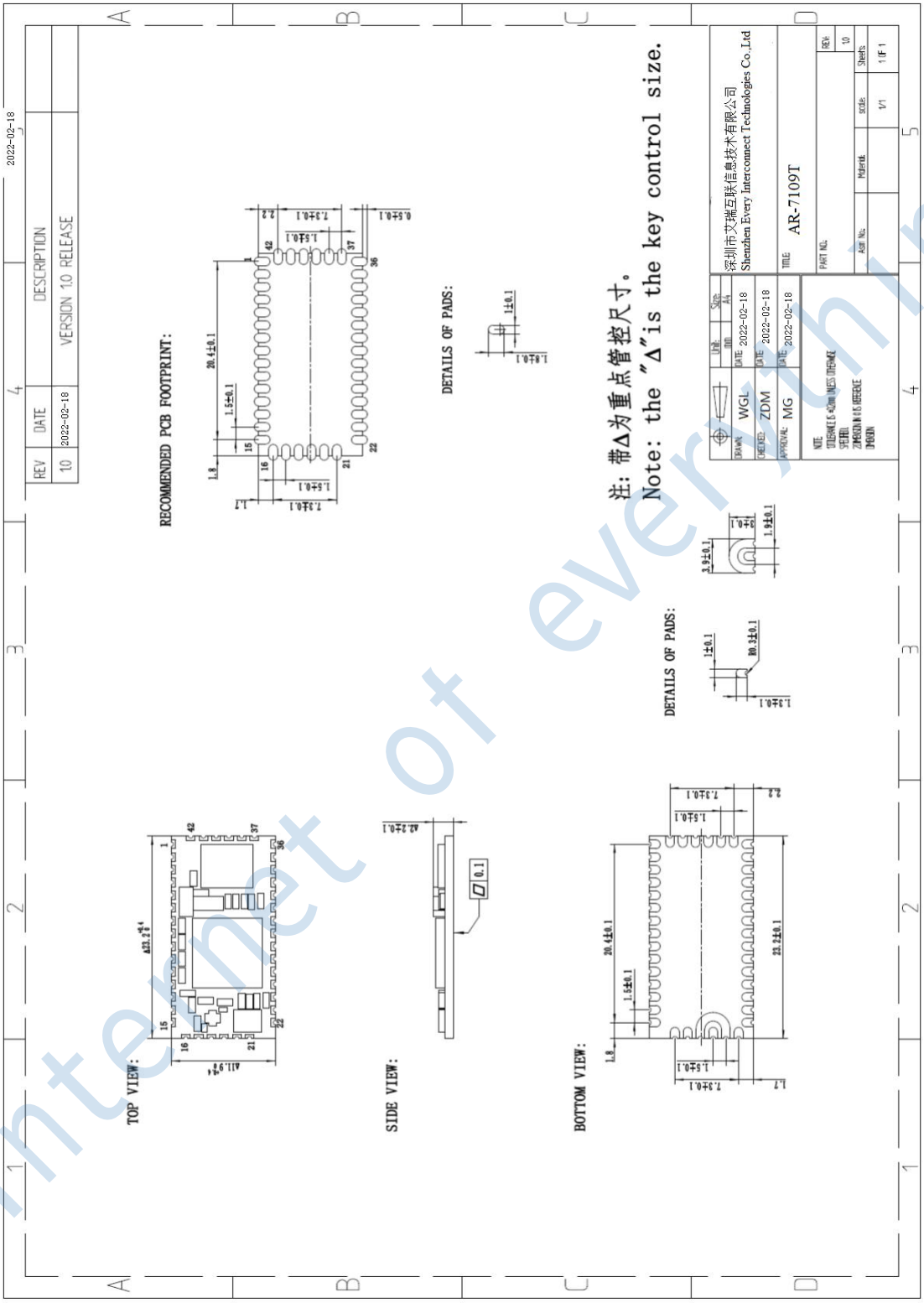
Digital-To-Analog Converter							
Parameter	**Conditions**			**Min**	**Typ**	**Max**	**Unit**
Resolution	_			_	_	16	Bits
Output sample rate, Fsample	_			8	_	48	kHz
SNR	fin=1 kHz B/W= 20Hz →20 kHz A- Weighted THD+N<0.1% 0dBFSinput	F_{sample}	Load				
		48kHz	100k0	_	95.4	_	dB
		48kHz	320	_	96.5	_	dB
		48kHz	160	_	95.8	_	dB
THD+N	fin=1 kHz B/W= 20Hz →20 kHz 0dBFSinput	F_{sample}	Load				
		8kHz	100k0	_	0.0021	_	%
		8kHz	320	_	0.0031	_	%
		8kHz	160	_	0.0034	_	%
		48kHz	100k0	_	0.0037	_	%
		48kHz	320	_	0.0029	_	%
		48kHz	160	_	0.0042	_	%
Digital gain	Digital gain resolution =1/32			-24	_	21.5	dB
Analog gain	Analog gain resolution =3 dB			-21	_	0	dB
Output voltage	Full-scale swing (differential)			_	_	778	mVrms
Stereo separation (crosstalk)				_	-90.5	_	dB

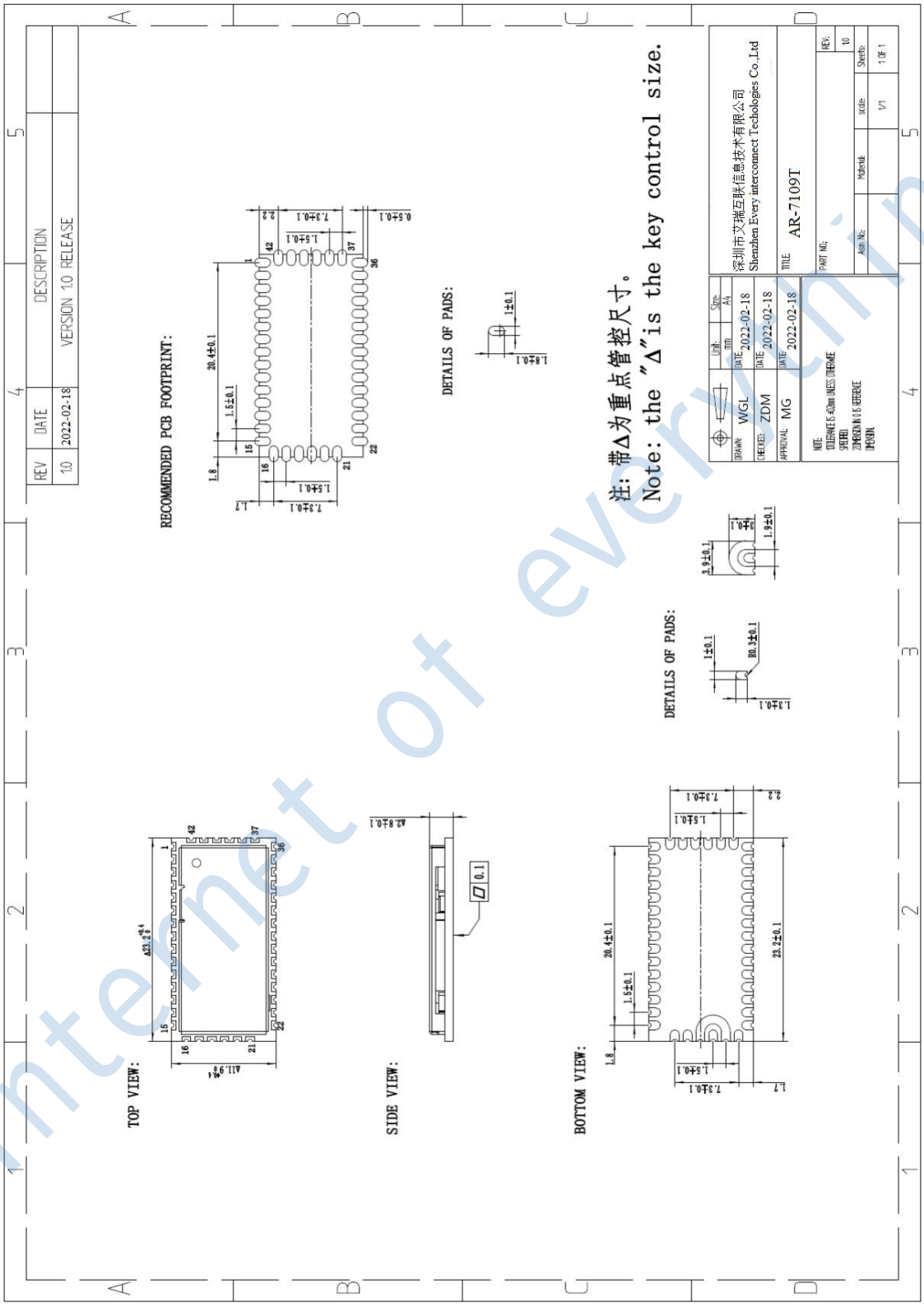
5.3.4 Microphone Bias Generator

Table 14: Microphone Bias Generator

Microphone Bias Generator	Min	Typ	Max	Unit
Output voltage (Tunable, step = 0.1 V)	1.5	_	2.1	V
Output current capability	0.07	_	3.0	mA
Output noise（B/W = 20 Hz → 20 kHz Unweighted）	4.5	5.1	7.3	uVrms
Crosstalk Between Microphones (Using recommended application circuit)	_	80	_	db
Load capacitance (From parasitic PCB routing and package	_	_	0.1	nf

6 Mechanical Characteristic





7 Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50 and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in figure 12 below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

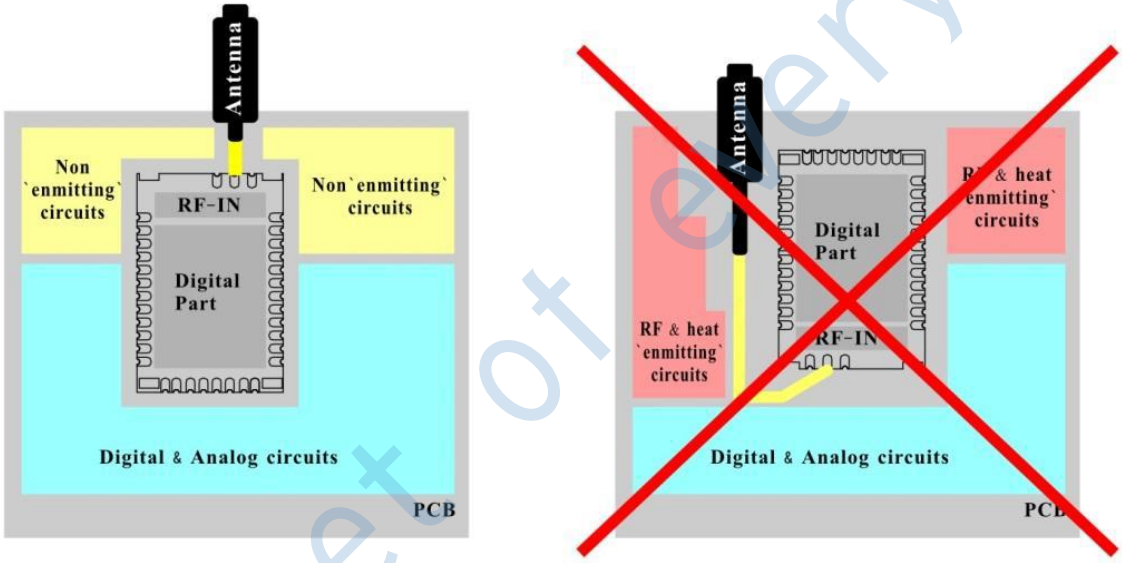


Figure 13: Placement the Module on a System Board

7.1 Input/output Terminal Characteristics

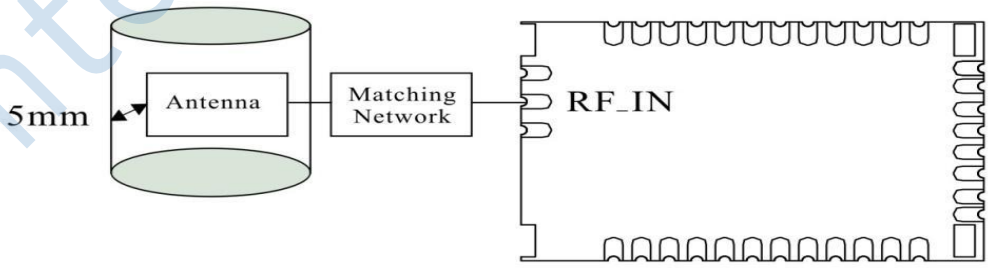


Figure 14: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

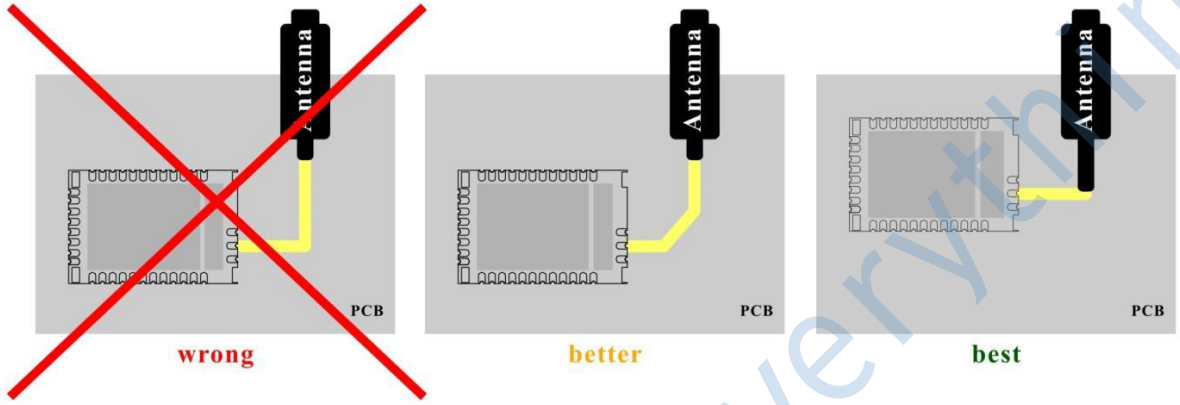


Figure 15: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

8 Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

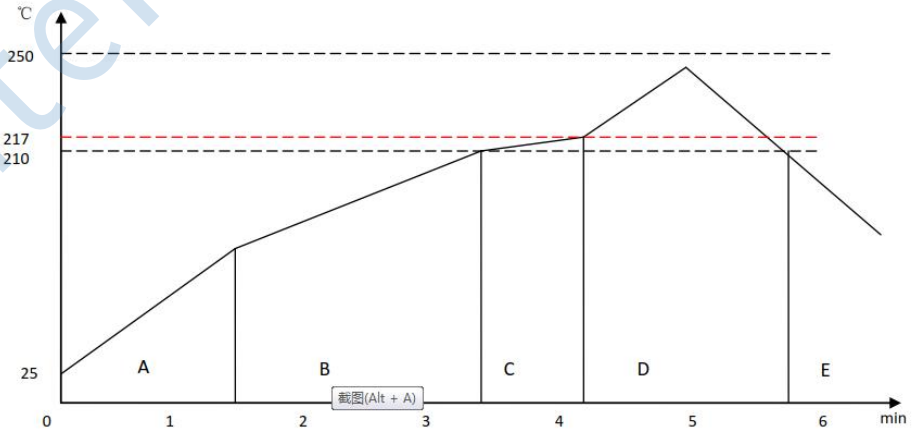


Figure 16: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 ℃. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

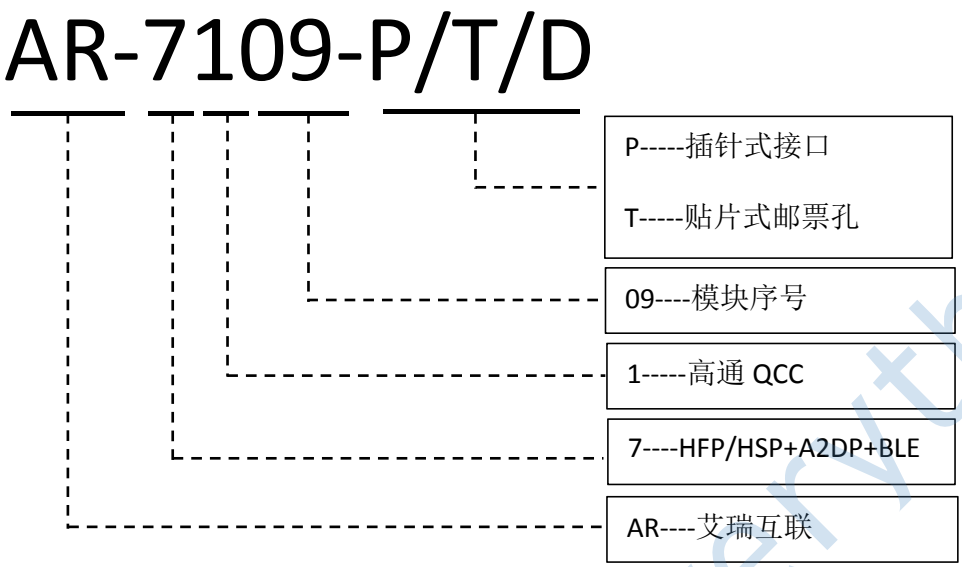
Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210 ° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250℃. The soldering time should be 30 to 90 second when the temperature is above 217℃.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4℃.**

9 Ordering Information



9.1 Module function

功能序号	产品主要功能	说明	备注
2	HID		
3	SPP 数传		
4	BLE 数传		
5	SPP+BLE 数传		
6	A2DP	仅音频	
7	HFP/HSP+A2DP+BLE	电话+音频+数传	全功能
8	WiFi		
9	Bluetooth+WiFi		

9.2 The chip manufacturer

厂家序号	芯片厂家	说明
1	高通 QCC	
2	中科蓝讯 AB	
3	杰理 JL	
4	锐迪科 RDA	
5	中芯微 WS	
6	TI	
7	NORDIC	
8	瑞昱 REALTEK	
9	南方硅谷	

9.3 Module mounting mode

序号	贴装方式	说明
1	P	插针式
2	T	邮票孔贴装
3	D	邮票孔+插针

IMPORTANT NOTICE

By Shenzhen Every Interconnect Technologies Co., Ltd (AR) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the AR terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

AR warrants performance of its products to specifications applicable at the time of sale in accordance with AR's standard warranty. Testing and other quality control techniques are utilized to the extent AR deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimize risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimize inherent or procedural hazards. AR products are not authorized for use as critical components in life support devices or systems without the express written approval of an officer of the company. Life support devices or systems are devices or systems that are intended for surgical implant into the body, or support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

AR assumes no liability for applications assistance or customer product design. AR does not warrant or represent that any license, either express or implied, is granted under any patent right, mask work right, or other intellectual property right of AR covering or relating or any combination, machine, or process in which such products or services might be or are used.