Production Information Data

Model: AR-7107T

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Shenzhen Every Interconnect Technologies Co., Ltd.

TEL: (0755)23410907

Fax: (0755)23410907

E-mail: guang.ma@every-connect.com

Add: 4 / F, building D, Guangming Zhizao hi tech Industrial Park,

Zhenmeicommunity, Xinhu street, Guangming District, Shenzhen

Release Record

Version	Release Date	Comments
V1.0	2022-02-15	Init

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1 Introduction

AR-7107T is a small form factor, low power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to design into fully certified embedded Bluetooth solutions.With EVERY's AT+™ programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such as HS/HF, A2DP, AVRCP, SPP,and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) ,BT5.0 and delivers up to 3 Mbps data rate for distances to 10M.The module is an appropriate product for designers who want to add wireless capability to their products.

1.1 Naming Declaration

Table 1: Naming Declaration

New Naming	Old Naming	Description
AR-7107T	NA	■ High-performance programmable Bluetooth® stereo audio SoC with Qualcomm® aptX™ audio mono codec ■ Tri-core processor architecture with low power for extended battery life ■ Qualcomm TrueWireless™ stereo earbuds

1.2 Block Diagram

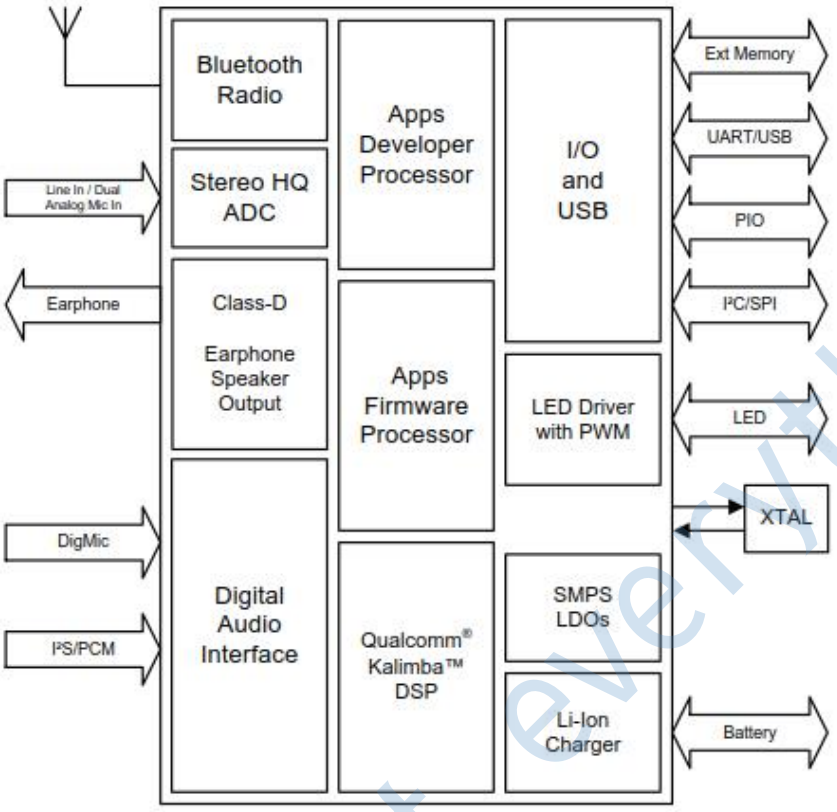


Figure 1: Block Diagram

1.3 Features

- Fully qualified single-chip dual mode Bluetooth v5.0
- 120 MHz Qualcomm® Kalimba™ audio DSP
- 32 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- Advanced audio algorithms
- High-performance 24‑bit audio interface
- Digital and analog microphone interfaces
- Flexible PIO controller and LED pins with PWM support
- 1 or 2-mic Qualcomm® cVc™ headset noise reduction and echo cancellation technology
- aptX mono, SBC, and AAC audio codecs support

- aptX, aptX HD, aptX Low Latency codecs individually supported under relative licensing fee
- Serial interfaces: UART, Bit Serializer (I²C/SPI),USB 2.0
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- 90-ball 5.5 x 5.5 x 1.0 mm, 0.5 mm pitch VFBGA

1.4 Applications

- Automobile hands-free applications
- Stereo headset applications
- Cable replacements
- Bar code and RFID scanners
- Measurement and monitoring systems
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

2 General Specification

Table 2: General Specification

Bluetooth Specification	
Standard	Fully qualified single-chip dual mode Bluetooth v5.0 , Class 1.5a
Chipset	QCC3020 VFBGA
Profiles	HS/HF, A2DP, AVRCP, SPP, etc. detailed profiles depends on the firmware
Frequency Band	2.402GHz ~ 2.480GHz
Maximum Data Rate	3Mbps
RF Input Impedance	50 ohms
Baseband Crystal OSC	26MHz
Interface	UART, PIO, AIO, USB, SPI, Speaker, Microphone, etc.
Sensitivity	-85dBm@0.1%BER
RF TX Power	7dBm
Power	
Supply Voltage	2.7V ~ 3.6V DC
Working Current	Depends on profiles
Standby Current	TBD
Operating Environment	

Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Certifications	TBD
Environmental	TBD
Dimension and Weight	
Dimension	12.5mm x 13.1mm x 0.8mm
Weight	TBD

a) The maximum RF TX Power is 9dBm.

3 Device details

3.1 Audio subsystem

■ 32‑bit Kalimba audio digital signal processor (DSP) core with flexible clocking from 2 MHz to 120 MHz to allow optimization and trade-off performance vs. power consumption

■ DSP runs from ROM

■ 80 KB program random access memory (RAM)

■ 256 KB data RAM

■ 5 Mb ROM

3.2 Application subsystem

■ Dual core application subsystem 32 MHz operation

■ 32‑bit Firmware Processor:

☐ Reserved for system use

☐ Runs Bluetooth upper stack, profiles, house-keeping code

■ 32‑bit Developer Processor:

☐ Runs developer applications

■ Both cores execute code from external flash memory using QSPI clocked at 32 MHz

■ On-chip caches per core allow for optimized performance and power consumption

Bluetooth subsystem

■ Qualified to Bluetooth v5.0 specification including 2 Mbps Bluetooth low energy

(Production parts)

■ Single ended antenna connection with on-chip balun and Tx/Rx switch

■ Bluetooth, Bluetooth low energy, and mixed topologies supported

■ Class 1 support

3.3 Li-ion battery charger

■ Integrated battery charger supporting up to 200 mA charge current

■ Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V

■ Thermal monitoring and management are implementable in application software

■ Pre-charge to fast charge transition configurable at 2.5 V,2.9 V, 3.0 V, and 3.1 V

3.4 Power management

■ Integrated power management unit (PMU) to minimize external components

■ QCC3020 VFBGA runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)

■ Auto-switching between battery and USB (or other) charging source

■ Power islands employed to optimize power consumption for variety of use-cases

■ Dual switch-mode power supply (SMPS):

☐ Automatic mode selection to minimize power consumption

☐ 1.8 V SMPS generates power for both the device and off-chip circuits

☐ Dedicated digital SMPS (output voltage changes automatically to minimize device power consumption)

3.5 Audio engine and digital audio interfaces

■ 1 x unidirectional 24‑bit I²S input

■ Differential high efficiency Class-D earphone speaker driver output:

☐ Class-D signal-to-noise ratio (SNR): 98.3 dBA typ.

☐ Class-D total harmonic distortion plus noise (THD+N): -87.5 dB typ.

■ Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs:

☐ SNR single-ended: 101 dBA typ.

☐ THD+N single-ended: -85 dB typ.

■ 1 microphone bias (single bias shared by the two channels):

☐ Crosstalk attenuation between two inputs using recommended application circuit: 80 dB typ.

■ Digital microphone inputs with capability to interface up to 6 digital microphones

■ Both analog-to-digital converter (ADC)s and the digital-to-analog converter (DAC) support sample rates of 8, 16, 32, 44.1, 48, 96 kHz. The DAC also supports 192 kHz.

3.6 Peripherals and physical interfaces

■ A UART interface

■ 2 x Bit Serializers (programmable serial peripheral interface (SPI) and I²C hardware accelerator)

■ 1 x USB interface:

☐ A full speed USB (USB-FS) Device (12 Mbps) – USB interface includes ESD protection to IEC-61000-4-2 (device level)

■ QSPI NOR flash interface

☐ QSPI encryption to protect developer code and data

☐ Encryption programmable with a 128‑bit security key of original equipment manufacturer (OEM) choice stored in on-chip one-time programmable (OTP) memory

■ Up to 20 PIO and 5 open drain/digital input LED pads with pulse width modulation (PWM)

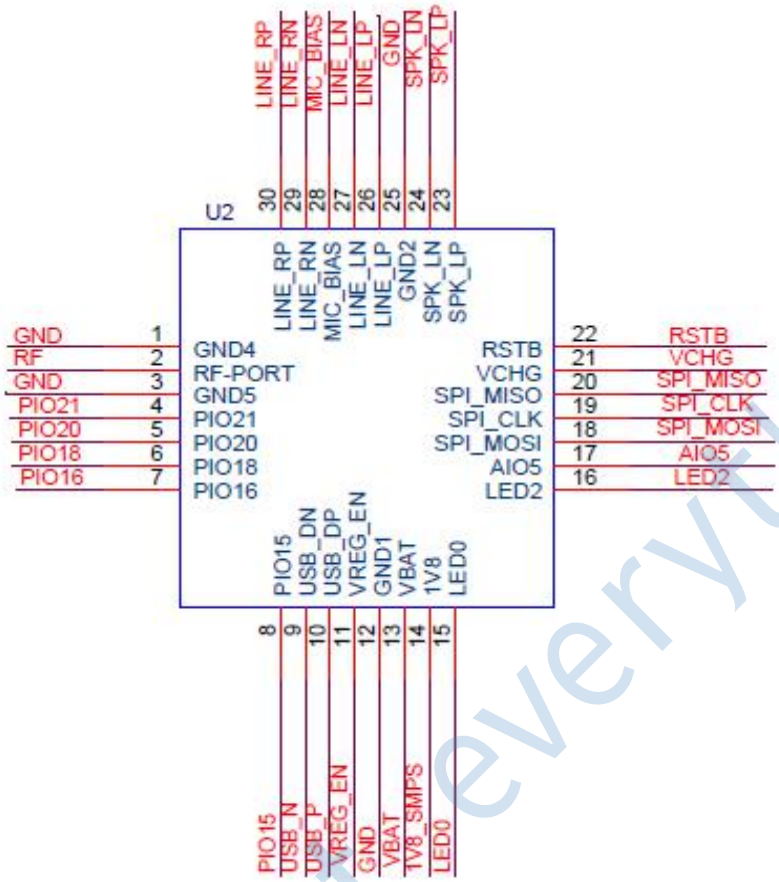
3.7 Package and compliance

■ 90-ball 5.5 x 5.5 x 1.0 mm, 0.5 mm pitch VFBGA

■ Green (restriction of hazardous substances (RoHS) compliant and no antimony or halogenated flame retardants)

4 Pin Definition

4.1 Pin Configuration



4.2 Pin Definition

Table 3: Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	RF	Analogue	Analogue Programmable input/output line
3	GND	Ground	Ground
4	PIO21	I/O	Bidirectional with weak pull-down Digital: Bidirectional with programmable strength internal pull-up/pull-down Programmable input/output line
5	PIO20	I/O	Bidirectional with weak pull-down Digital: Bidirectional with programmable strength internal pull-up/pull-down Programmable input/output line
6	PIO18	I/O	Bidirectional with weak pull-down Digital: Bidirectional with programmable strength internal pull-up/pull-down Programmable input/output line
7	PIO16	I/O	Bidirectional with weak pull-down Digital: Bidirectional with programmable strength internal pull-

			up/pull-down Programmable input/output line
8	PIO15	I/O	Bidirectional with weak pull-down Digital: Bidirectional with programmable strength internal pull-up/pull-down Programmable input/output line
9	USB_N	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
10	USB_P	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
11	VREG_EN	I	Regulator enable input.Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
12	GND	Ground	Ground
13	VBAT	Supply	Battery voltage input.
14	1V8_SMPS	Analog	Inductor connection for 1.8 V SMPS.
15	LED0	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
16	LED2	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
17	AIO5	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
18	SPI_MOSI	Bidirectional with Strong pull-down	SPI_MISO: Debug SPI data input Alternative function: -I2S_SD_IN:I²S synchronous data input
19	SPI_CLK	Bidirectional with Strong pull-down	SPI_CLK: Debug SPI clockAlternative function: -I2S_SCK:I²S synchronous data clock
20	SPI_MISO	Bidirectional with Strong pull-down	SPI_MISO: Debug SPI data output Alternative function: - I2S_SD_OUT:I²S synchronous data output
21	VCHG	Analogue	Charger input sense pin.
22	RSTB	Input with strong pull-up	Reset if low. Pull low for minimum 5ms to cause a reset.
23	SPK_LP	Analogue	Headphone/speaker differential output, positive.Alternative function:Differential line output, positive
24	SPK_LN	Analogue	Headphone/speaker differential output, negative.Alternative function:Differential line output, negative
25	GND	Analogue	Analogue
26	LINE_LP	Analogue	Microphone differential 1 input, positive.Alternative function:Differential audio line input left,positive
27	LINE_LN	Analogue	Microphone differential 1 input, negative.
28	MIC_BIAS	Analogue	Mic bias output.
29	LINE_RN	Analogue	Microphone differential 2 input, negative.Alternative function:Differential audio line input right,negative

30	LINE_RP	Analogue	Microphone differential 2 input, positive.Alternative function:Differential audio line input right,positive

5 Physical Interfaces

5.1 RESETB

AR-7107T is reset from several sources:

- RESETB pin
- Power-on reset
- Software configured watchdog timer
- UART break character

The RESETB pin is an active low reset. Assert the reset signal for a period > 5 ms to ensure a full reset.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

5.1.1 Digital Pin States on Reset

Table 4 shows the pin states of AR-7107T on reset.

Table 4: Pin Status on Reset

Pin Name / Group	I/O Type	Reset
USB_DP	Digital bidirectional	Tristate
USB_DN	Digital bidirectional	Tristate
PIO0	Digital bidirectional	Strong PU
PIO1	Digital bidirectional	Strong PD
PIO2	Digital bidirectional	Strong PD
PIO3	Digital bidirectional	Strong PD
PIO4	Digital bidirectional	Strong PU
PIO5	Digital bidirectional	Strong PD
PIO6	Digital bidirectional	Strong PD
PIO7	Digital bidirectional	Strong PD

5.2 Automatic Reset Protection

AR-7107T includes an automatic reset protection circuit that restarts the AR-7107T when an unexpected reset occurs, for example, ESD strike or lowering of RST#. This reset protection circuit automatically restarts the AR-7107T and enables the application to restore previous operation.

NOTE If RESETB is held low for > 2.4 s and VDD is not applied, AR-7107T turns off. A rising edge on VDD is then required to power on AR-7107T.

5.3 Serial Interfaces

5.3.1 USB Interface

AR-7107T has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices.

The USB interface on AR-7107T acts as a USB peripheral, responding to requests from a master host controller.

AR-7107T contains internal USB termination resistors and requires no external resistors.

AR-7107T supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification).

5.3.2 UART Interface

AR-7107T has a UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug.

When AR-7107T is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.

UART configuration parameters, such as baud rate and packet format, are set using the AR-7107T firmware.

NOTE: To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

The use of UART and USB are mutually exclusive.

Table 5: Possible UART Settings

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 6 lists common baud rates and their associated error values for PSKEY_UART_BITRATE. To set the UART baud rate, load PSKEY_UART_BITRATE with the number of bits per second.

Table 6: Standard Baud Rates

Baud rate	PS Key value(bits per second)	Error
1200	1200	1.73%
2400	2400	1.73%
4800	4800	1.73%
9600	9600	-0.82%
19200	19200	0.45%
38400	38400	-0.18%
57600	57600	0.03%
76800	76800	0.14%
115200	115200	0.03%
230400	230400	0.03%
460800	460800	-0.02%
921600	921600	0.00%
1382400	1382400	-0.01%
1843200	1843200	0.00%
2764800	2764800	0.00%
3686400	3686400	0.00%

5.3.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

5.4 Audio Interface

5.4.1 Audio Codec Interface

The interface provides following features:

- Mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band

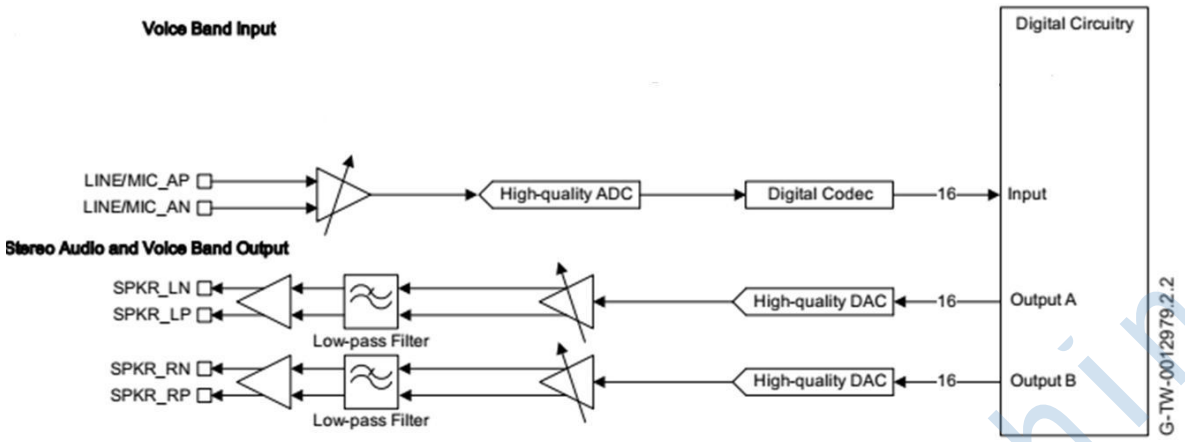


Figure 3: Audio Input and Output

The AR-7107T audio codec uses a fully differential architecture in the analog signal path. This architecture results in low common-mode-noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. The module features a differential stereo audio output interfaces.

5.4.1.1 ADC

The ADC has a second-order Sigma-Delta converter.
The ADC is a separate channel with identical functionality.
Each channel has an analog and a digital gain stage.

5.4.1.2 ADC Sample Rate Selection

ADC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz，48Khz.

5.4.1.3 ADC Audio Input Gain

The audio input gain consists of the following components:
An analog gain stage based on a pre-amplifier and an analog gain amplifier.
A digital gain stage.

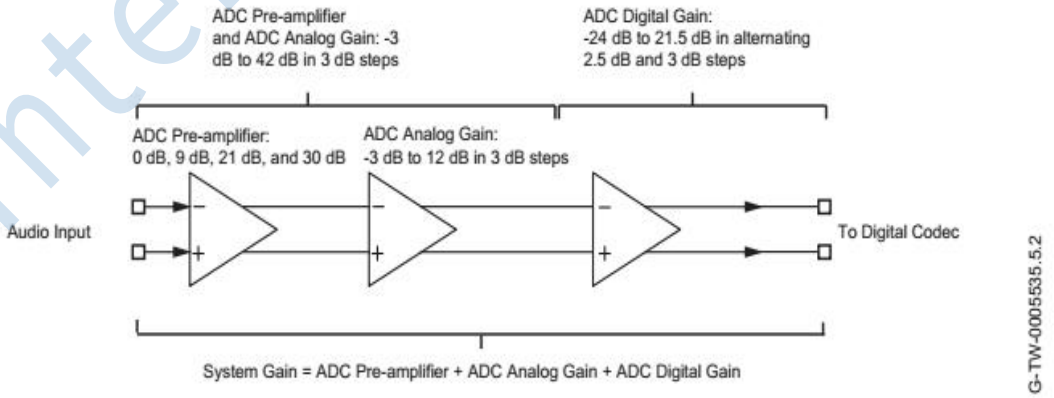


Figure 4: Audio Input Gain

5.4.1.4 ADC Pre-Amplifier And Analog/Digital Gain

The gain of the ADC inputs can be configured in the range of -27 dB to 63.5 dB steps, making it suitable for line and microphone input levels. 0 dB is 1600 mV pk-pk input.

The ADC input impedance is nominal 6 kΩ except when 0 dB pre-amplifier gain is selected when it becomes 12 kΩ.

If the input pre-amplifier is disabled, the input impedance varies between 6 k and 34 k depending on gain selection. In normal operation, the input pre-amplifier is enabled.

Calls connected by the VM stream automatically select the distribution of gain within the ADC for best performance. Alternatively, the individual gain stages can be set.

5.4.1.5 ADC Digital Gain

Table 7: ADC Audio Input Gain Selection

Digital Gain Selection Value	ADC Digital Gain Setting(Db)	Digital Gain Selection Value	ADC Digital Gain Setting(Db)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

5.4.1.6 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

A long IIR filter suitable for music (> 44.1 kHz).G.722 filter. This is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance. This filter is the best selection for 8 kHz/16 kHz/voice.

5.4.1.7 DAC

The DAC consists of two high-quality DACs:

Each DAC has a fourth-order Sigma-Delta converter.

Each DAC is a separate channel with identical functionality.

Each channel has an analog and a digital gain stage.

5.4.1.8 DAC Sample Rate Selection

DAC supports the following sample rates: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz，48Khz.

5.4.1.9 DAC Gain

The DAC outputs have two gain stages, a digital stage followed by an analog stage. The digital gain varies between -24 dB and 21.5 dB and the analog gain between 0 dB and -21 dB, giving a total range of -45 dB to 21.5 dB.

Calls connected by the VM stream automatically select the distribution of gain within the DAC for best performance. Alternatively, the individual gain stages can be set.

Table 8: DAC Digital Gain Selection

Digital Gain Selection Value	DAC Digital Gain Setting (Db)	Digital Gain Selection Value	DAC Digital Gain Setting (Db)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5

Table 9: DAC Analog Gain Selection

Analog gain selection value	DAC analog gain setting (dB)	Analog gain selection value	DAC analog gain setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

5.4.1.10 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default long FIR filter for best performance at ≥ 44.1 kHz.
- A short FIR to reduce latency.
- A narrow FIR (a sharp roll-off at Nyquist) for G.722 compliance. Best for 8 kHz/16 kHz.

5.4.1.11 Microphone Bias Generator

AR-7107T contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones.

Figure 5 shows a typical biasing circuit for electret condenser microphones..

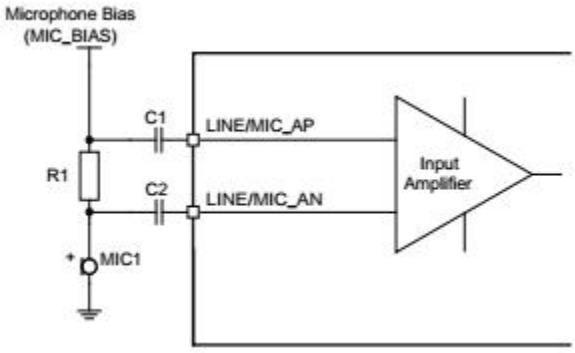


Figure 5: Micro phone Biasing

The microphone bias generator provides a selectable output voltage of 1.8 V or 2.6 V nominal.

No output capacitor is required.

5.4.1.12 Output Stage

The output stage digital circuitry converts the signal from 16 bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analog output circuitry.

class AB output stage amplifier.

Figure 6 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

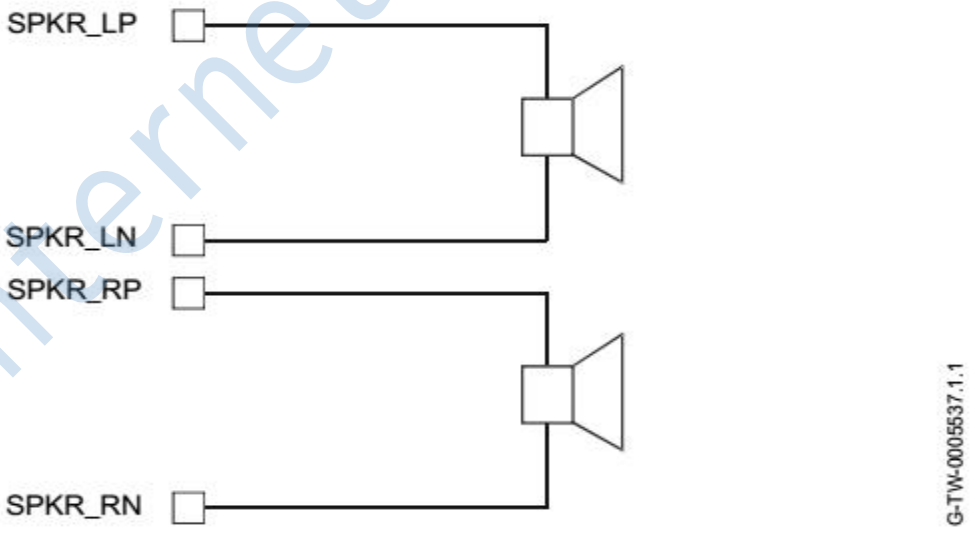


Figure 6: Speaker Output

5.4.1.13 Mono Operator

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

5.4.1.14 Sidetone

In some applications, it is necessary to implement sidetone. This sidetone function applies configurable gain to the microphone signal and feeds it into the DAC stream. The sidetone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface

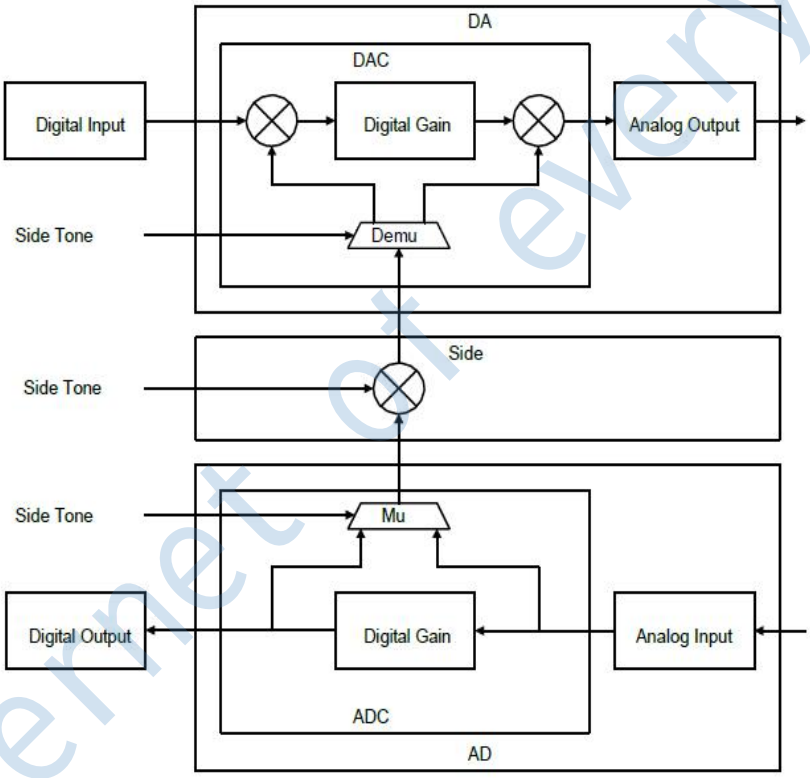


Figure 7: Sidetone

The ADC provides simple gain to the sidetone data. The gain values range from -32.6 dB to 12.0 dB in alternating steps of 2.5 dB and 3.5 Db

Table 10: Sidetone Gain

Value	Sidetone Gain(dB)	Value	Sidetone Gain(dB)
0	-32.6	8	-8.5
1	-30.1	9	-6.0

2	-26.6	10	-2.5
3	-24.1	11	0
4	-20.6	12	3.5
5	-18.1	13	6.0
6	-14.5	14	9.5
7	-12.0	15	12.0

5.4.1.15 Integrated Digital IIR Filter

AR-7107T has a programmable digital filter integrated into the ADC channel of the codec.

The filter is a 2-stage, second-order IIR and is for functions such as custom wind noise reduction.

The filter also has optional DC blocking.

The filter has 10 configuration words in this order:

• 1 for gain value

• 8 for coefficient values (b01, b02, a01, a02, b11, b12, a11, a12)

• 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit two's complement signed integer with the format NN.NNNNNNNNN.

NOTE The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

5.4.2 I2S Interface

AR-7107T supports I²S input and output via its industry-standard I²S digital audio interface.

AR-7107T also supports several alternative PCM data formats. When in PCM mode, the following pin name to function mappings apply.

I²S Pin	PCM Function
I2Sn_SD_IN	PCM_IN
I2Sn_SD_OUT	PCM_OUT
I2Sn_WS	PCM_SYNC
I2Sn_SCK	PCM_CLK

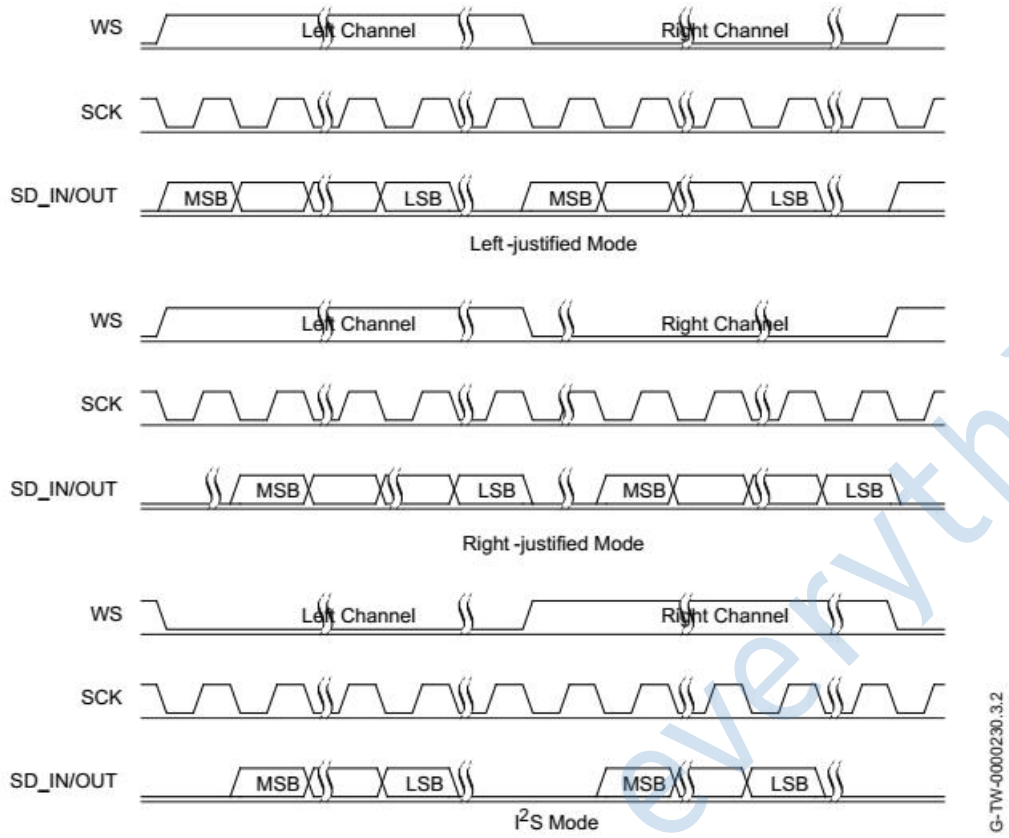


Figure 8: Digital Audio Interface Modes

The internal representation of audio samples within the AR-7107T QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Table 11: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
_	SCK Frequency	_	_	6.2	kHz
_	WS Frequency	_	_	96	kHz
T_{ch}	SCK high time	80	_	_	Ns
T_{ch}	SCK low time	80	_	_	Ns

Table 12: I²S Slave Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	_	_	Ns
t_{sh}	SCK high to WS invalid hold time	2.5	_	_	Ns
t_{opd}	SCK low to SD_OUT valid delay time	_	_	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	_	_	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	_	_	ns

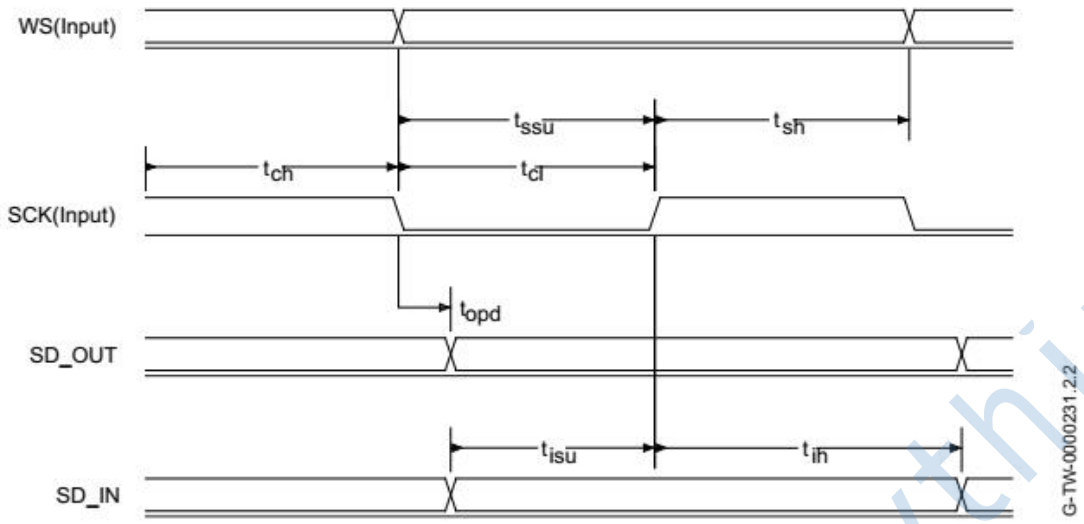


Figure 9: Digital Audio Interface Slave Timing

Table 13: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
_	SCK Frequency	_	_	6.2	MHz
_	WS Frequency	_	_	96	kHz

Table 14: I²S Master Mode Timing Parameters, WS And SCK As Outputs

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	_	_	39.27	ns
t_{opd}	SCK low to WS valid delay time	_	_	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	_	_	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	_	_	ns

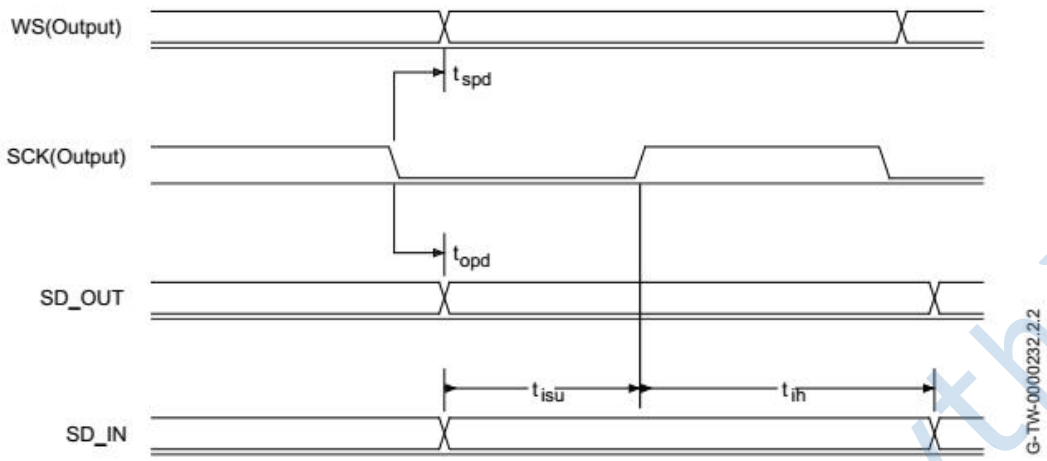


Figure 10: Digital Audio Interface Master Timing

5.4.3 aptx Codec

The aptX audio codec is available for high-quality stereo audio over Bluetooth. When incorporated in Bluetooth A2DP stereo products, aptX audio coding delivers full wired audio quality. The aptX audio codec source material is delivered transparently over the Bluetooth link, whether it is stored uncompressed or in an alternative compression (AAC, FLAC) format.

The aptX codec has the following target applications:

■ Bluetooth stereo headphones/headsets
■ Bluetooth automotive audio
■ Bluetooth stereo speakers

The aptX codec has the following benefits:

■ Outstanding Bluetooth Stereo audio quality
■ Faithful reproduction of full audio bandwidth
■ Minimization of lip-sync issues via low-delay audio decoding techniques
■ Nondestructive transcoding from other standard coded audio formats
■ Low code memory and data memory requirements
■ A2DP-compliant negotiation back to the SBC codec when connecting with legacy audio sources

The aptX codec has the following key features:

■ Multiple audio sample rate support, including Fs = 44.1 kHz and Fs = 48 kHz
■ Conveyance of CD-quality audio (16-bit and Fs = 44.1 kHz) over Bluetooth at a data rate of 352 kbps
■ Frequency response maintained from 10 Hz to 22 kHz for Fs = 48 kHz
■ Algorithmic delay less than 1.89 ms for Fs = 48 kHz
■ Dynamic range for 16-bit audio in excess of 92 dB

5.5 LED Drivers

AR-7107T includes two 3-pad synchronised PWM LED drivers for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

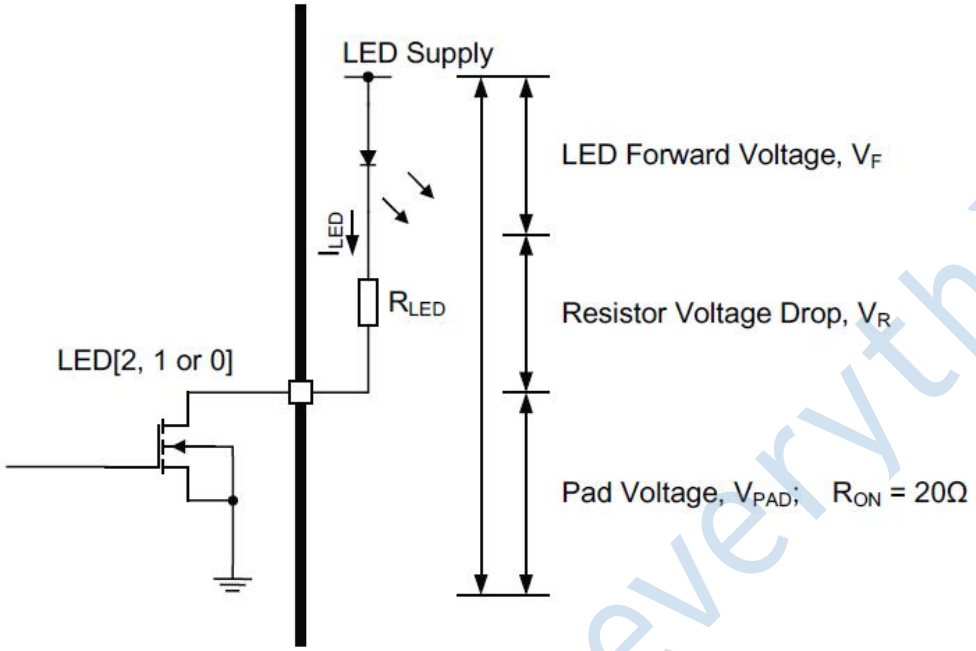


Figure 11: LED Equivalent Circuit

From Figure 3 it is possible to derive Equation 1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{V_{SUPPLY} - V_F}{R_{LED} + R_{ON}}$$

Equation 1: LED Current

For the LED pads to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, VR, keeps V_{PAD} below 0.5V. Equation 2 also applies.

$$V_{SUPPLY} = V_F + V_R + V_{PAD}$$

Equation 2: LED PAD Voltage

Note:

The LED current adds to the overall current. Conservative LED selection extends battery life.

5.6 RF Interface

The module integrates a filter. The user can connect a 50ohms antenna directly to the RF port.

5.7 General Purpose Analogue IO

The general purpose analog IO can be configured as ADC inputs by software. Do not connect it if not use.

5.8 General Purpose Digital IO

There are eight general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

6 Electrical Characteristic

6.1 Absolute Maximum Rating

Table 15: Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+85	° C
PIO/AIO Voltage	-0.4	3.60	V
VDD	-0.4	3.60	V
USB_DP/USB_DN Voltage	-0.4	3.60	V
Other Terminal Voltages except RF	-0.4	3.60	V

6.2 Recommended Operating Conditions

Table 16: Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	_	+85	° C
Operating Temperature Range	-40	_	+85	° C
VDD	+3.1	+3.3	+3.6	V
PIO	+1.7	+1.8	+3.6	V

6.3 Input/output Terminal Characteristics

6.3.1 Digital Terminals

Table 17: Digital Terminal

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.4	_	+0.4	V
VIH input logic level high	0.7VDDIO	_	VDDIO+0.4	V
Tr/Tf	_	_	25	ns

Output Voltage Levels				
VOL output logic level low, lOL = 4.0mA	_	_	0.4	V
VOH output logic level high, lOH = -4.0mA	VDDIO-0.2	_	_	V
Tr/Tf	_	_	5	ns
Input and Tri-state Current				
With strong pull-up	-150	-40	-10	µA
With strong pull-down	10	40	150	µA
With weak pull-up	-5	-1.0	-0.33	µA
With weak pull-down	0.33	+1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA
CI Input Capacitance	1.0	_	5.0	pF

VDDIO is the supply domain for this i/o. Typical value is 1.8V.

6.3.2 USB

Table 18: USB Terminal

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
VIL input logic level low	_	_	0.3VDD	V
VIH input logic level high	0.7VDD	_	_	V
Output Voltage Levels to Correctly Terminated USB Cable				
VOL output logic level low	0.0	_	0.2	V
VOH output logic level high	2.8	_	VDD	V

6.3.3 Stereo Codec: Analog-To-Digital Converter

Analog-To-Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	_		_	_	16	Bits
Input sample rate,Fsample	_		8	_	48	kHz
Maximum ADC input signal amplitude	0dB =1600 mVpk-pk		13	_	2260	mVpk-pk
SNR	fin=1 kHz B/W=20Hz→Fsample/2(20kHz max) A- Weighted THD+N<0.1% 1.6Vpk-pk input	F_{sample}				
		8 kHz	_	94.4	_	dB
		16 kHz	_	92.4	_	dB
		32 kHz	_	92.5	_	dB
		44.1 kHz	_	93.2	_	dB

		48 kHz	_	91.9	_	dB
THD+N	fin= 1 kHz B/W=20Hz→Fsample/2 (20 kHz max) 1.6Vpk-pk input	F_{sample}				
		8 kHz	_	0.004	_	%
		48 kHz	_	0.016	_	%
Digital gain	Digital gain resolution = 1/32	-24	_	21.5	_	dB
Analog gain	Pre-amplifier setting =0 dB, 9dB, 21dB or 30 dB Analog setting =-3dB to12 dBin 3dB steps	-3	_	42	_	dB
Stereo separation (crosstalk)			_	-89.9	_	dB

6.3.4 Stereo Codec: Digital-To-Analog Converter

Digital-To-Analog Converter							
Parameter	Conditions			Min	Typ	Max	Unit
Resolution	_			_	_	16	Bits
Output sample rate, Fsample	_			8	_	48	kHz
SNR	fin=1 kHz B/W= 20Hz →20 kHz A- Weighted THD+N<0.1% 0dBFSinput	F_{sample}	Load				
		48kHz	100k0	_	95.4	_	dB
		48kHz	320	_	96.5	_	dB
		48kHz	160	_	95.8	_	dB
THD+N	fin=1 kHz B/W= 20Hz →20 kHz 0dBFSinput	F_{sample}	Load				
		8kHz	100k0	_	0.0021	_	%
		8kHz	320	_	0.0031	_	%
		8kHz	160	_	0.0034	_	%
		48kHz	100k0	_	0.0037	_	%
		48kHz	320	_	0.0029	_	%
		48kHz	160	_	0.0042	_	%
Digital gain	Digital gain resolution =1/32			-24	_	21.5	dB
Analog gain	Analog gain resolution =3 dB			-21	_	0	dB
Output voltage	Full-scale swing (differential)			_	_	778	mVrms
Stereo separation (crosstalk)				_	-90.5	_	dB

6.3.5 Microphone Bias Generator

Microphone Bias Generator	Min	Typ	Max	Unit

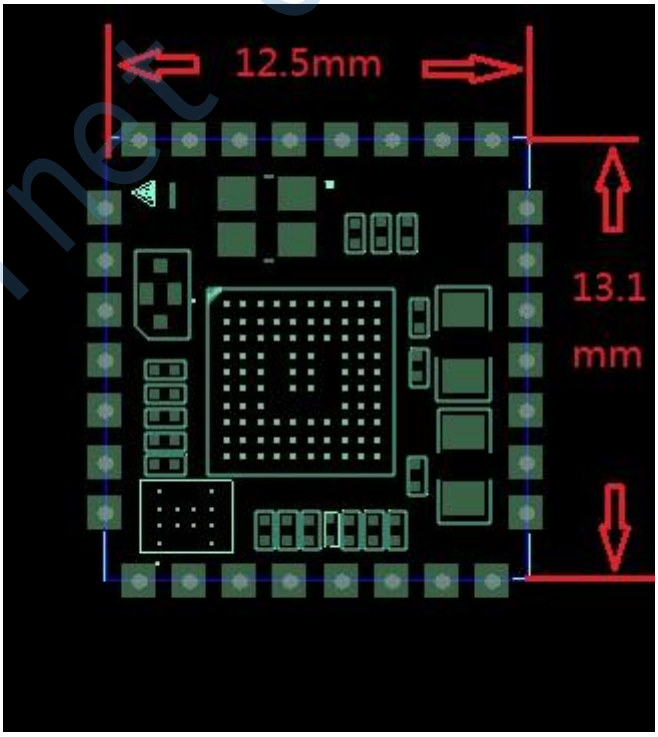
Output voltage (1.8 V selected)	1.62	1.8	1.98	V
Output voltage (2.6 V selected)	2.34	2.6	2.86	V
Drop out from VBAT input	_	_	300	mV
Output current available	_	_	2.8	mA
Minimum load for stated performance	70	_	_	uA

6.3.6 Currenta

Mode	Current(Ma)		
	Min	Type	Max
Limbo(Sleep)	_	1	_
Limbo(Idle)	_	4.8	_
Connectable(Idle)	_	TBD	_
Discoverable	_	TBD	_
Connected	_	10.5	_
Activecall	_	15.5	_

a:The current is related to the firmware version.

7 Reference Design



8 Recommended PCB Layout and Mounting Pattern

Placement and PCB layout are critical to optimize the performances of a module without on-board antenna designs. The trace from the antenna port of the module to an external antenna should be 50 and must be as short as possible to avoid any interference into the transceiver of the module. The location of the external antenna and RF-IN port of the module should be kept away from any noise sources and digital traces. A matching network might be needed in between the external antenna and RF-IN port to better match the impedance to minimize the return loss.

As indicated in figure 12 below, RF critical circuits of the module should be clearly separated from any digital circuits on the system board. All RF circuits in the module are close to the antenna port. The module, then, should be placed in this way that module digital part towards your digital section of the system PCB.

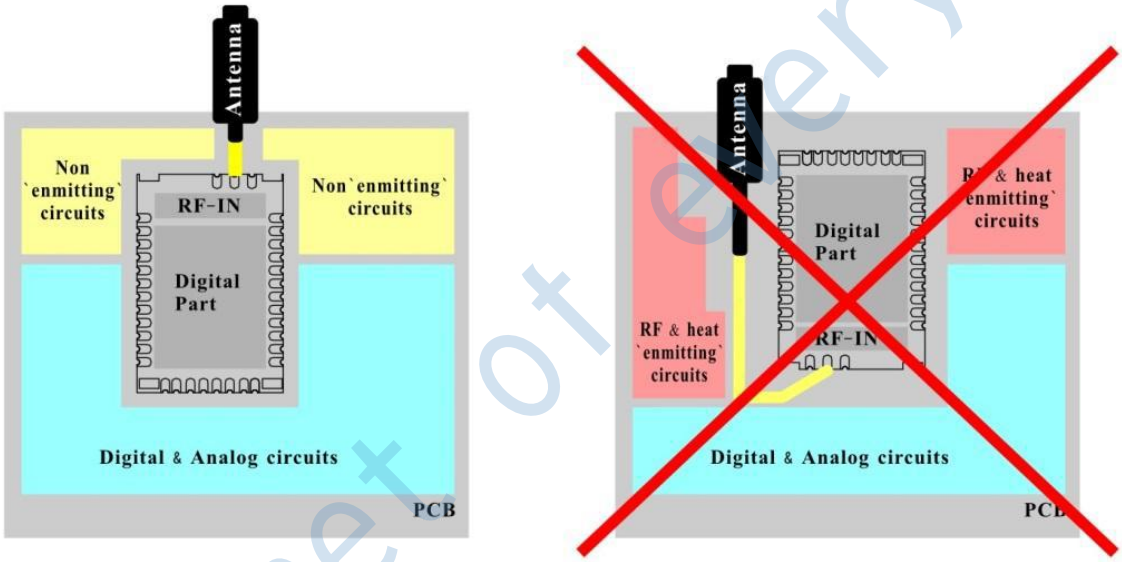


Figure 12: Placement the Module on a System Board

8.3 Input/output Terminal Characteristics

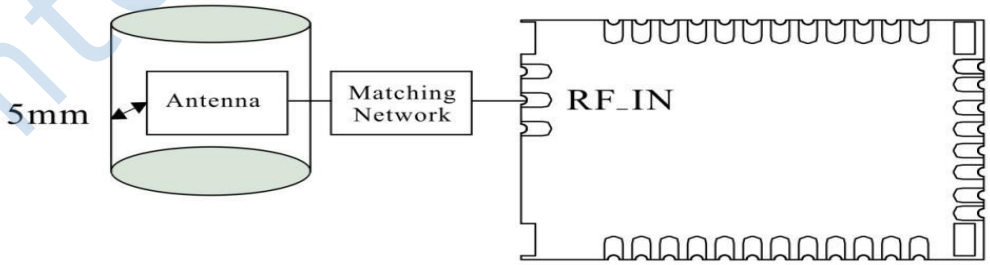


Figure 13: Leave 5mm Clearance Space from the Antenna

General design recommendations are:

- The length of the trace or connection line should be kept as short as possible.
- Distance between connection and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF close to digital sections of the system board should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

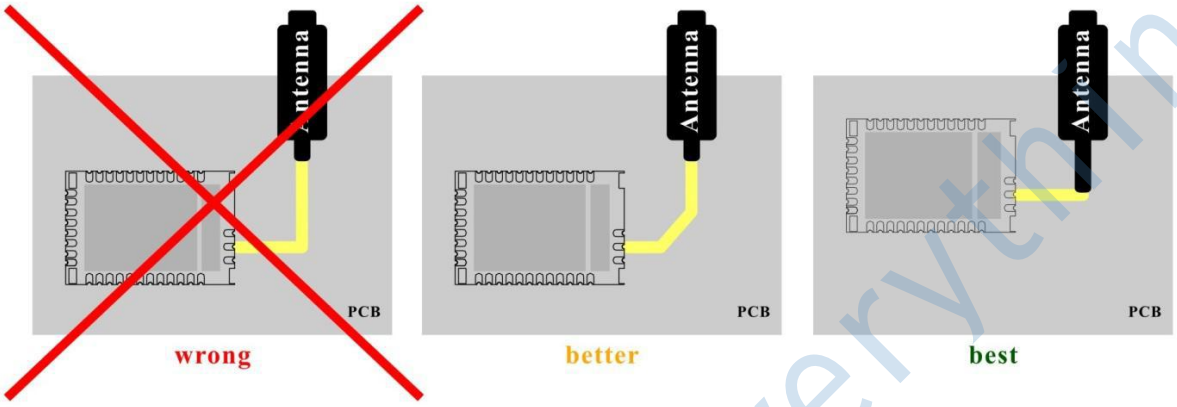


Figure 14: Recommended Trace Connects Antenna and the Module

- Routing of the RF-connection underneath the module should be avoided. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small and has huge tolerances. Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.

9 Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

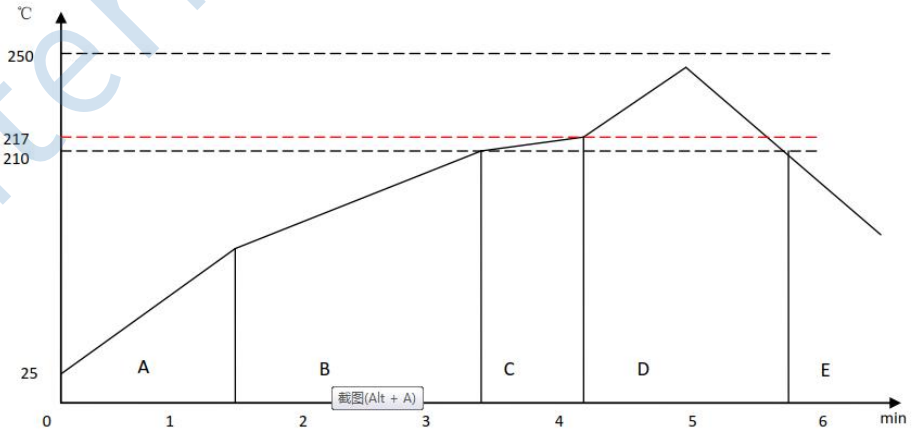


Figure 15: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2**

C/s. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 ℃. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board.

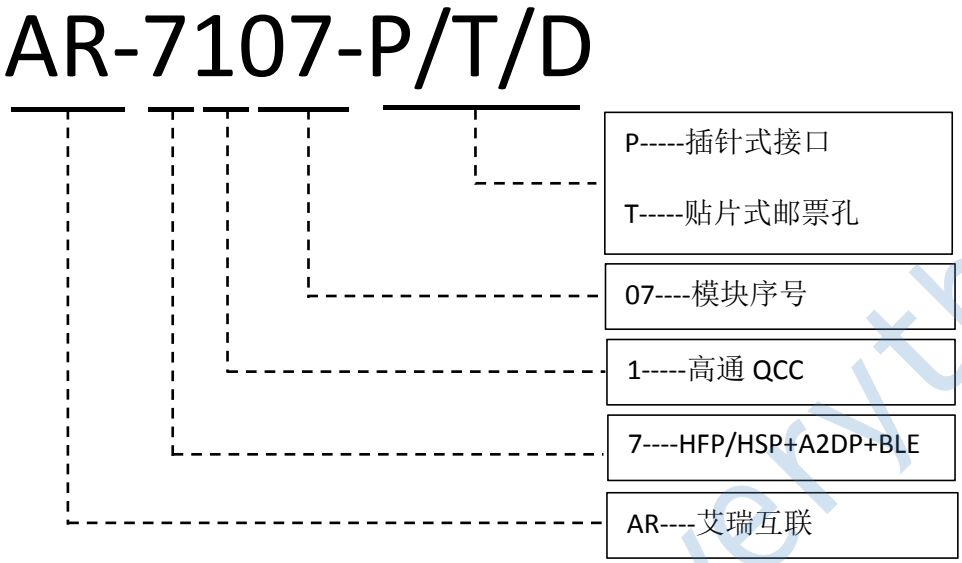
The temperature is recommended to be 150° to 210 ° for 60 to 120 second for this zone.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250℃. The soldering time should be 30 to 90 second when the temperature is above 217℃.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4℃.**

10 Ordering Information



10.1 Module function

功能序号	产品主要功能	说明	备注
2	HID		
3	SPP 数传		
4	BLE 数传		
5	SPP+BLE 数传		
6	A2DP	仅音频	
7	HFP/HSP+A2DP+BLE	电话+音频+数传	全功能
8	WiFi		
9	Bluetooth+WiFi		

10.2 The chip manufacturer

厂家序号	芯片厂家	说明
1	高通 QCC	
2	中科蓝讯 AB	
3	杰理 JL	
4	锐迪科 RDA	
5	中芯微 WS	
6	TI	
7	NORDIC	
8	瑞昱 REALTEK	
9	南方硅谷	

10.3 Module mounting mode

序号	贴装方式	说明
1	P	插针式
2	T	邮票孔贴装
3	D	邮票孔+插针

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